

Degas Schematics

Bay Trail - D

2016-05-18

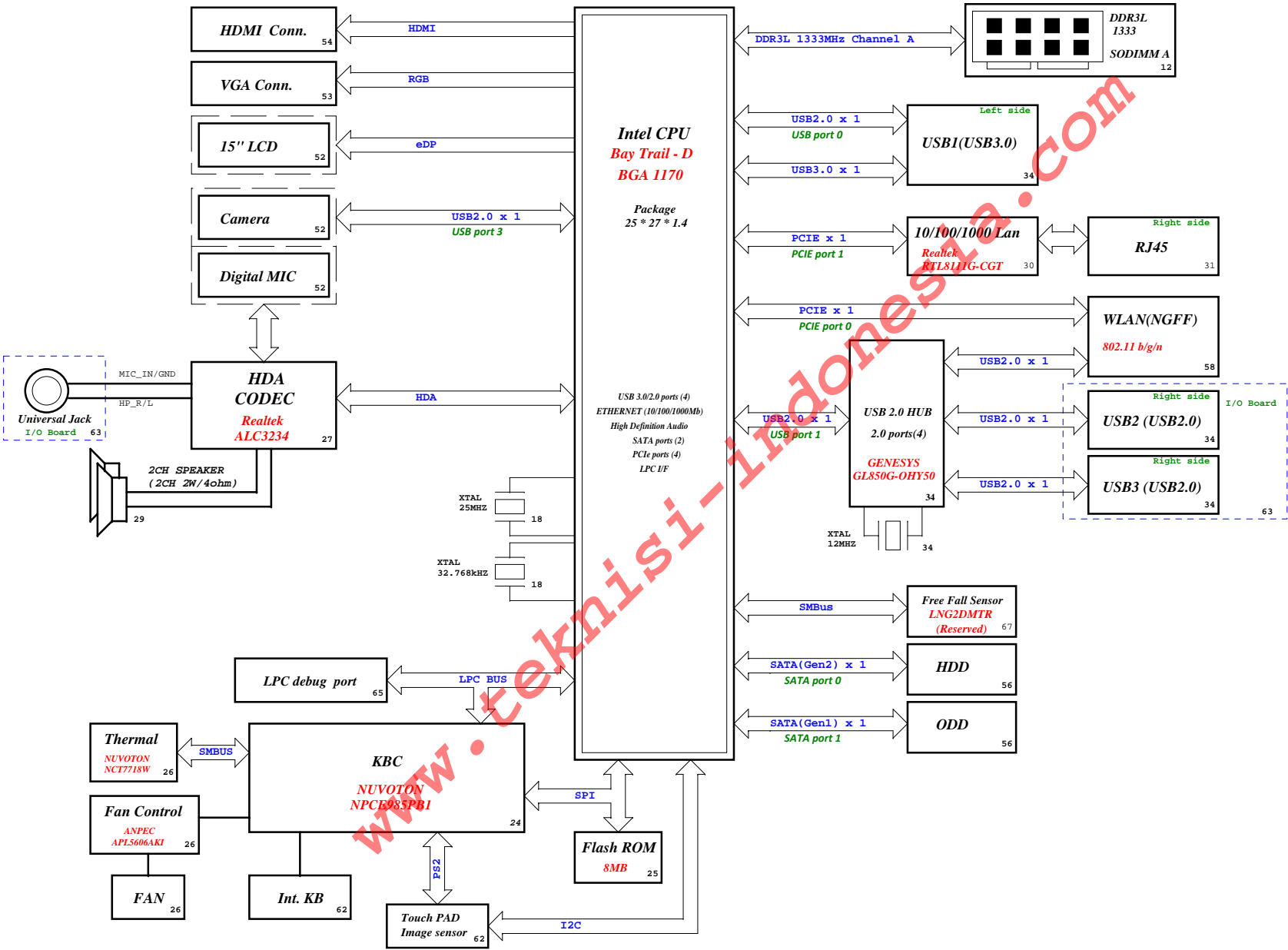
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DY : None Installed

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Cover Page			
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Degas Bay Trail-D Block Diagram



CHARGER	
BQ24727RGRR-1-GP	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95833HRTZ-GP	46, 47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0
CPU 1.0V	
SY8206DQNC	50
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5
CPU 1.05V	
RT8068AZQW	50
INPUTS	OUTPUTS
3D3V_S5	1D05V_S0
System LDO 1.8V	
S-1339D18-M5T1U3-GP51	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5
System LDO 1.5V	
S-1339D15-M5001-GP	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
System switches	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
1D8V_S5	1D8V_S0
1D35V_S3	1D35V_S0
1D0V_S5	1D0V_S0
PCB LAYER	
L1:Top L2:GND L3:Signal L4:Signal L5:VCC L6:Bottom	


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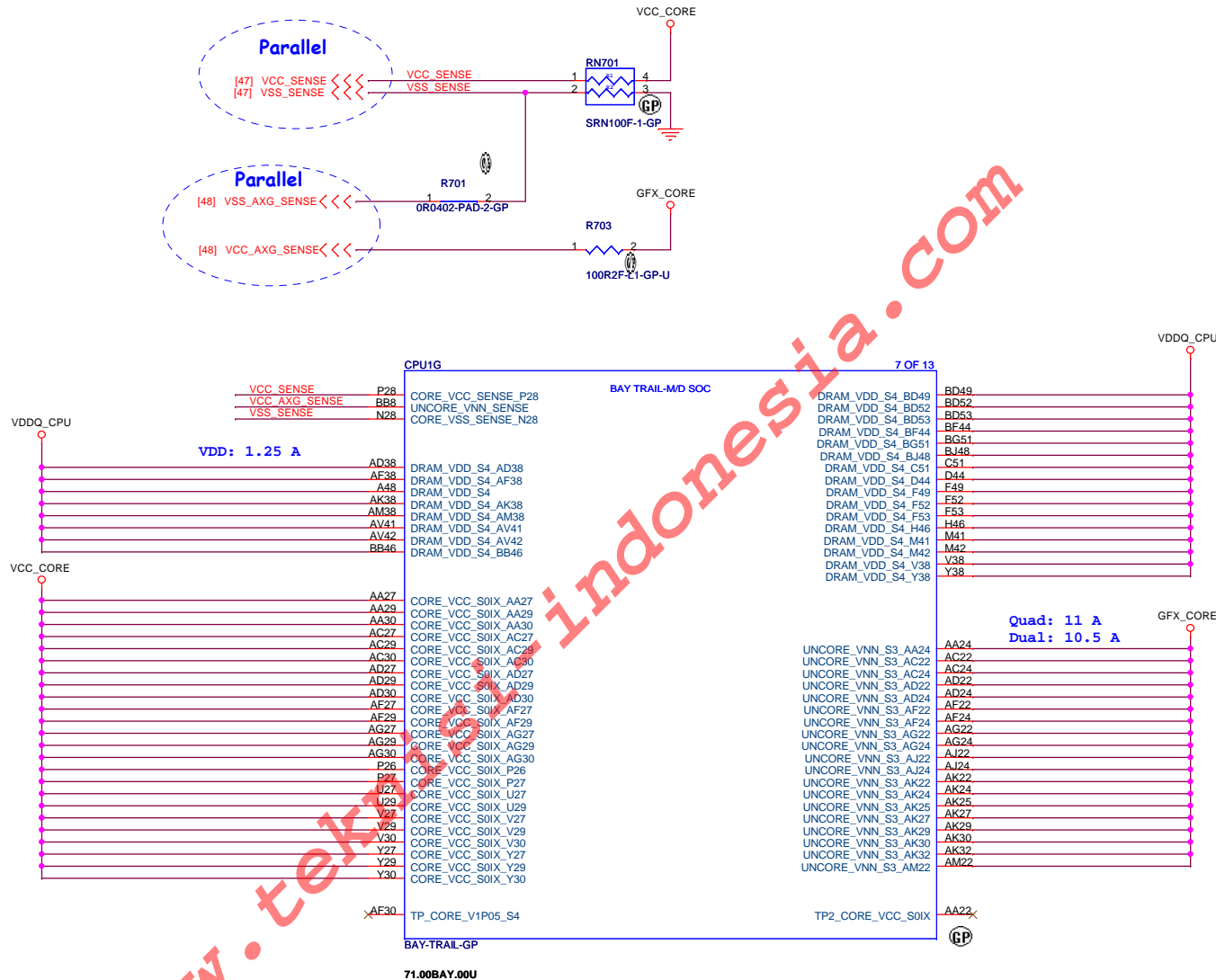
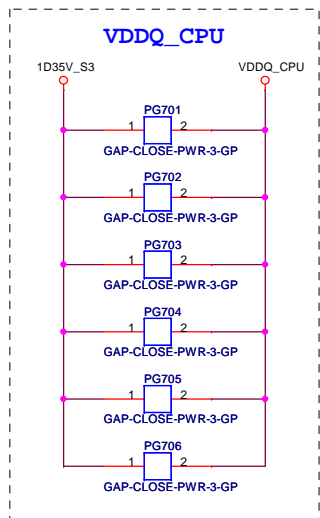
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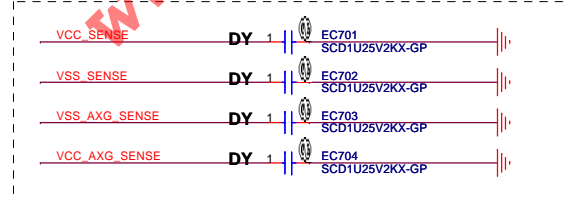
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EMI Caps



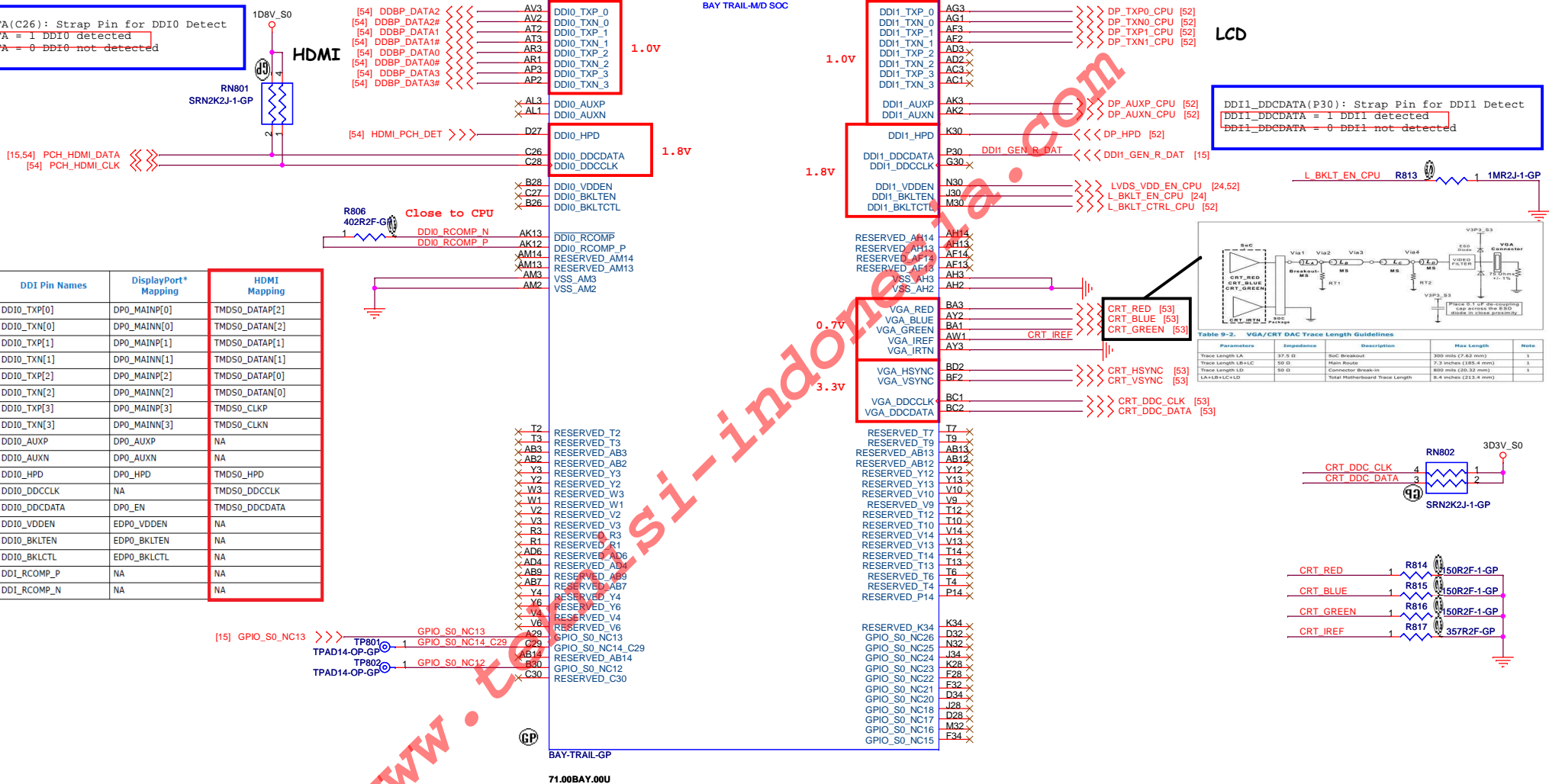
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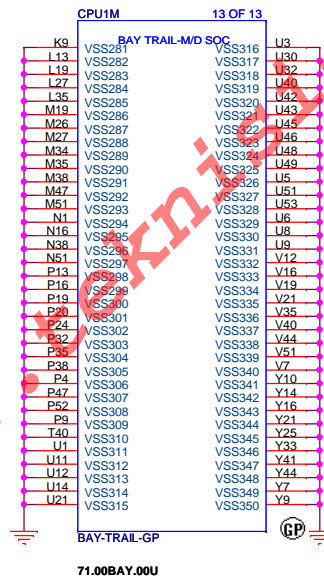
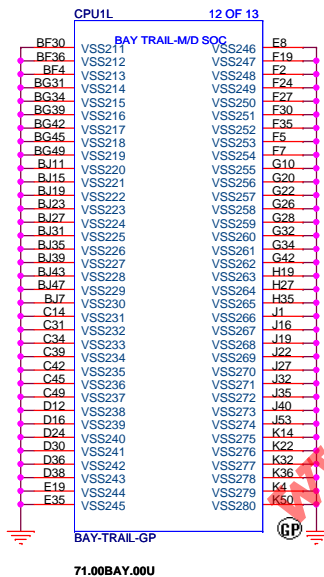
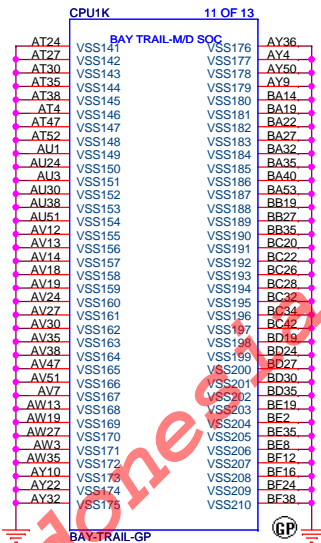
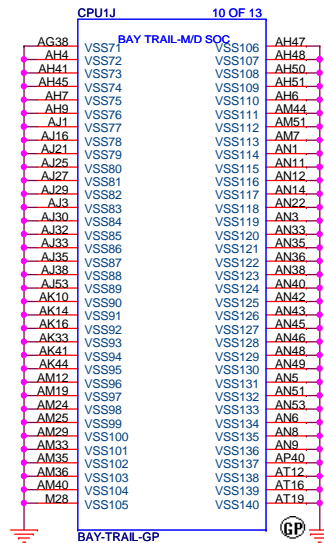
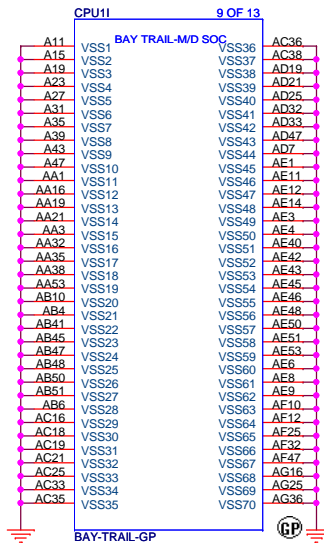
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DDI0_DDCDATA(C26): Strap Pin for DDI0 Detect
DDI0_DDCDATA = 1 DDI0 detected
DDI0_DDCDATA = 0 DDI0 not detected

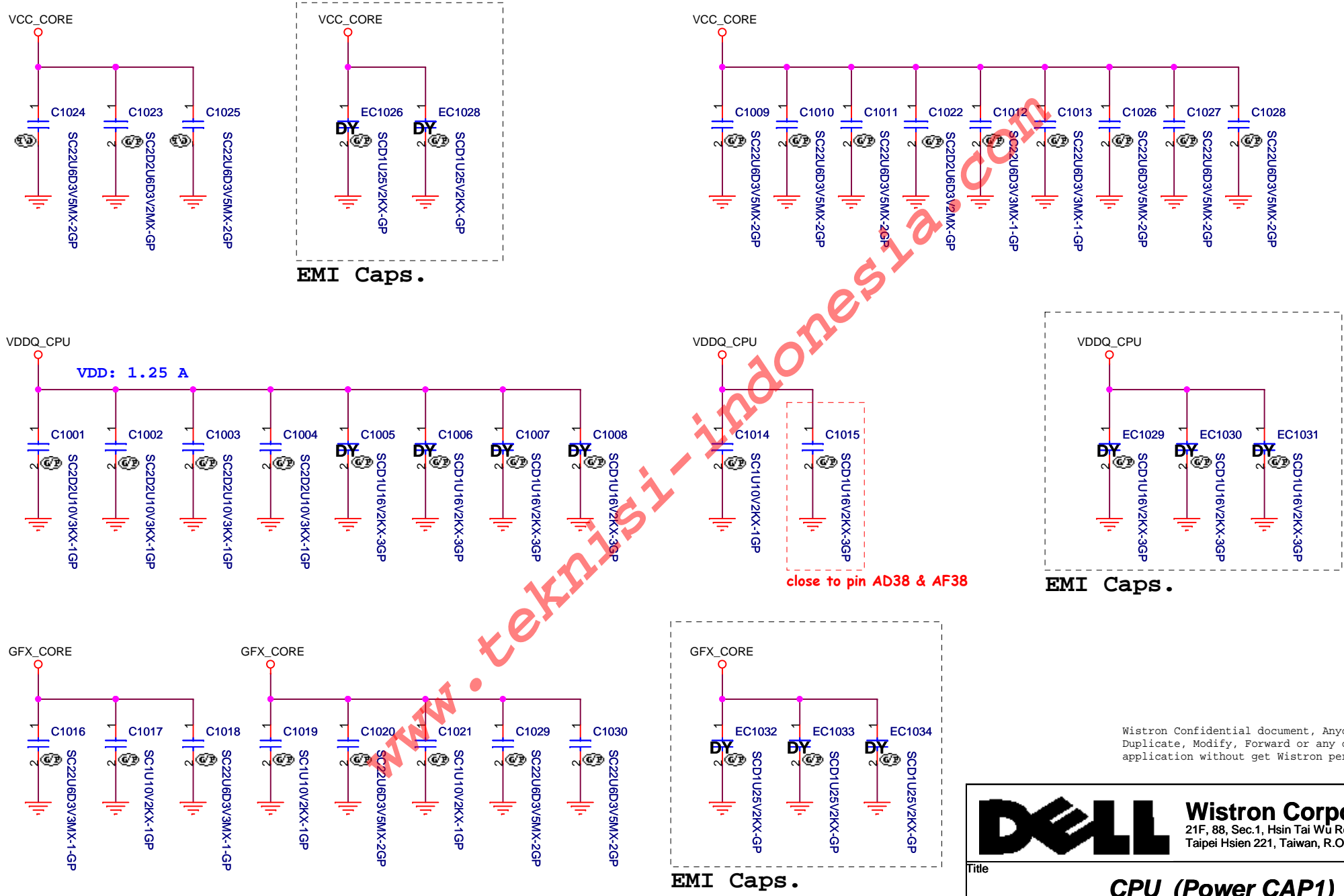


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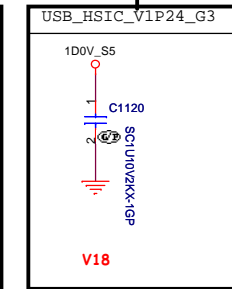
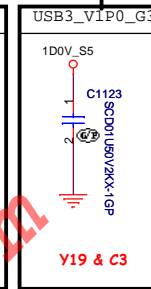
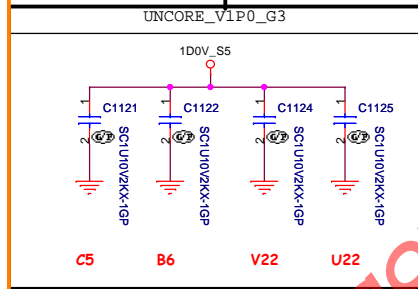
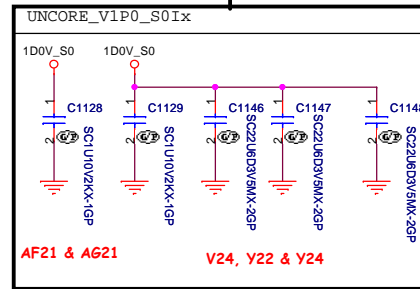
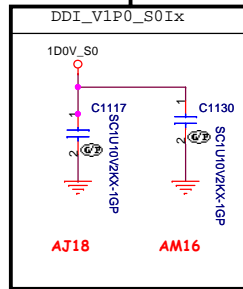
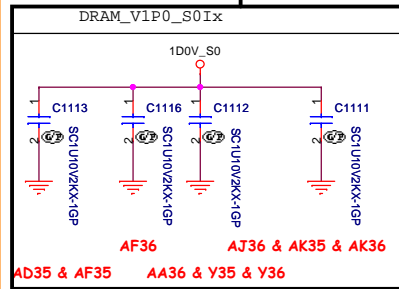
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Main Func = CPU

VLP0Sx: 2.1 A

VLP0A: 0.35 A

VLP24A: 0.035 A

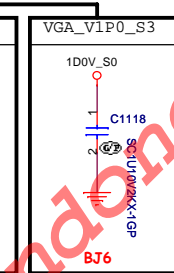
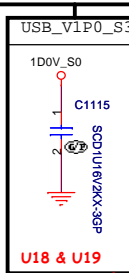
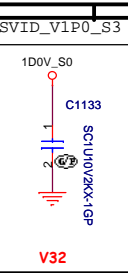
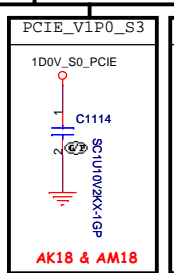
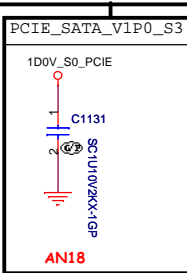
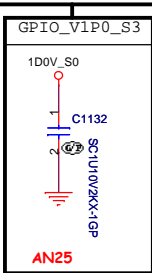
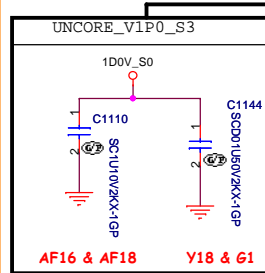


V18: USB_HSIC_VLP24_G3 pin(s) can be connected to VLP0A platform rail if USB HSIC is not used.

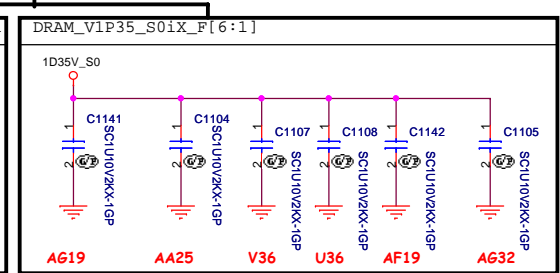
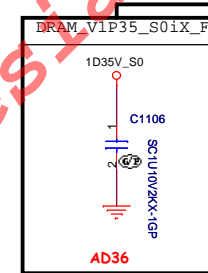
2A change

VLP0S: 0.9 A

VLP35Sx (VSFR): 0.4 A



2A change

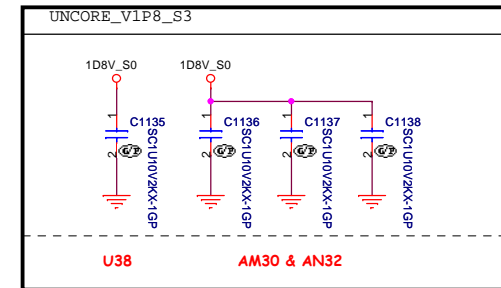
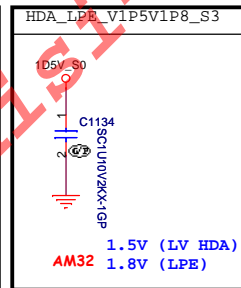
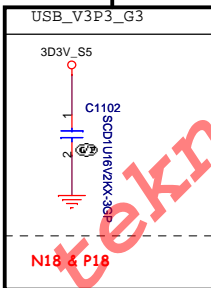
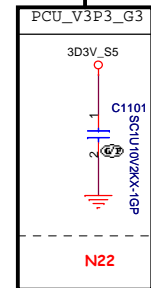
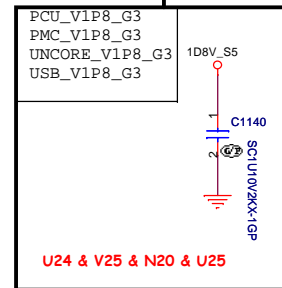
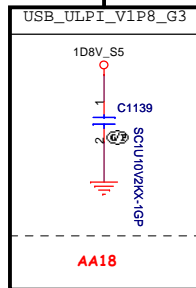


VLP8A: 0.065 A

V3P3A: 0.055 A

VLP5VLP8S (VAUD):
See VLP8S

VLP8S: 0.01 A

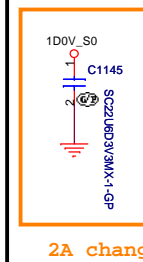
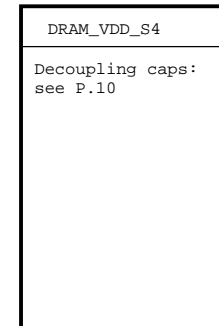
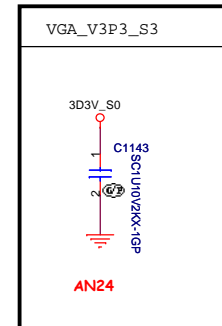
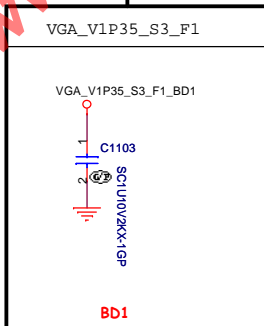
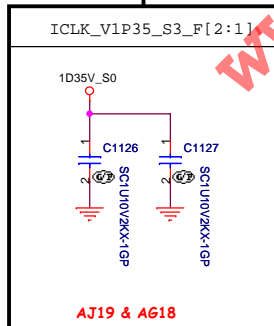
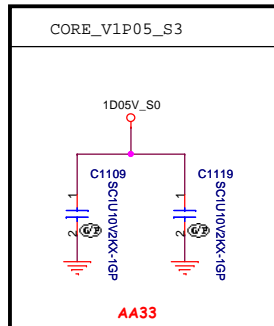


VLP0S5: 1.1 A

VLP35S: 0.045 A

V3P3S: 0.03 A

VDD: 1.25 A




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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap (A16 Override)
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI (Default)	Normal Operation (Default)	DDI0 detected	DDI1 detected	DDI1 detected	Top address bit is unchanged (Default)
Low	LPC	Override	DDI0 not detected (Default)	DDI1 not detected (Default)	DDI1 not detected	Top address bit is inverted

Table 20. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[056]	Legacy	1b	PMC_CORE_PWROK de-asserted	Top Swap (A16 Override) 0 = Top address bit is inverted 1 = Top address bit is unchanged
GPIO_S0_SC[063]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[065]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

INTEL BTM EDS Rev2.5

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

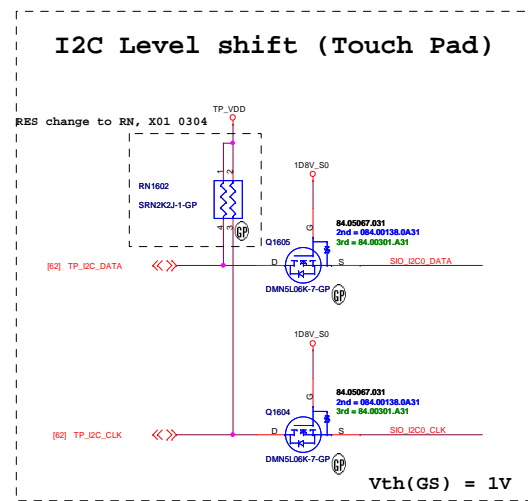
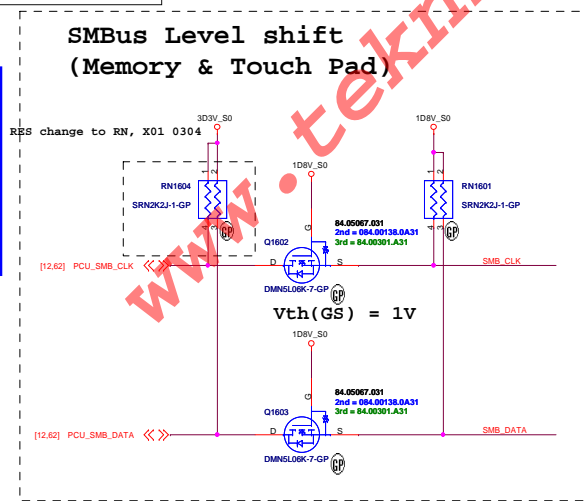
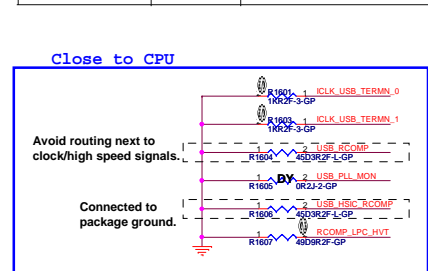
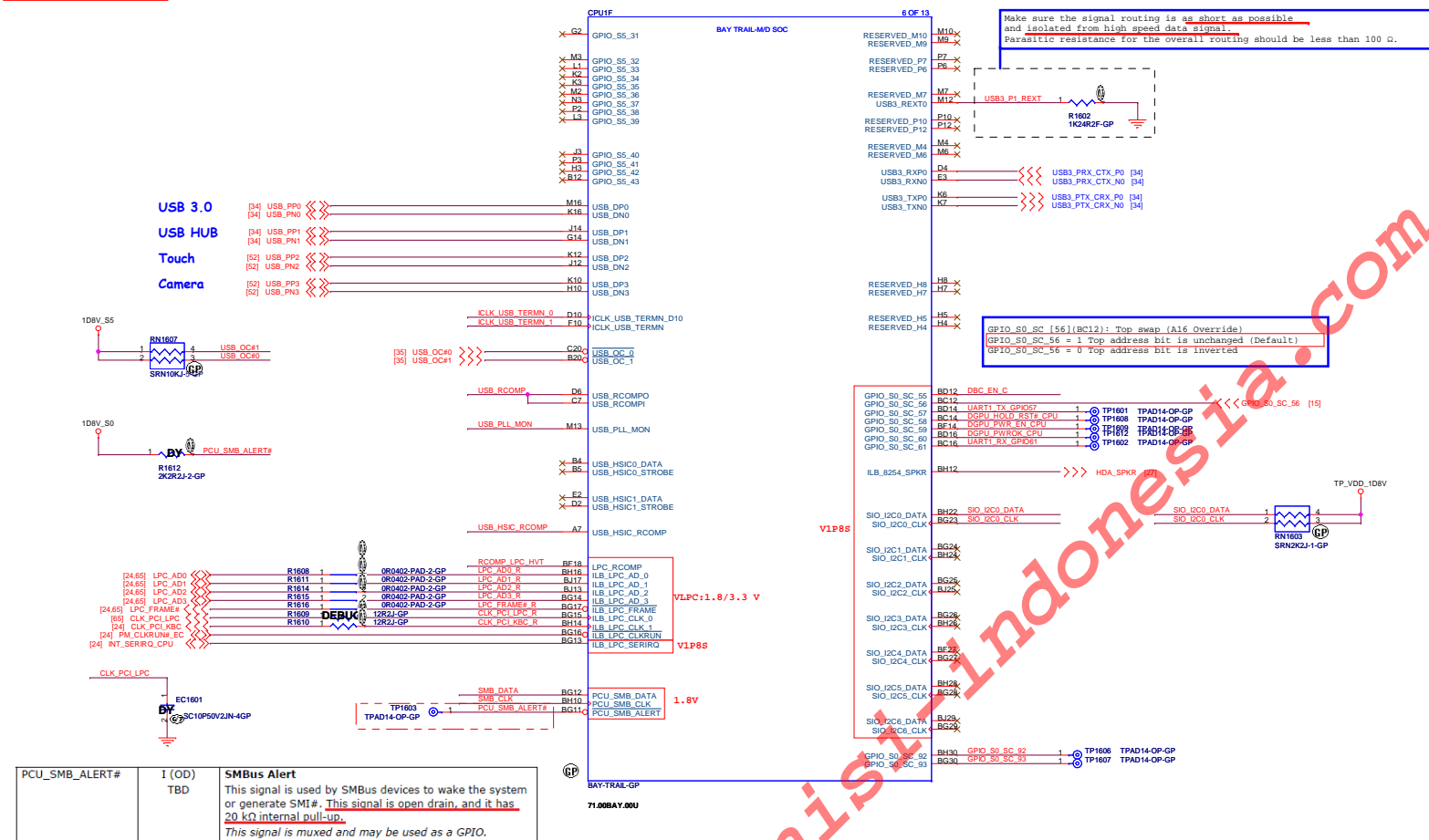
Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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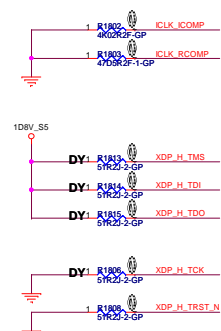
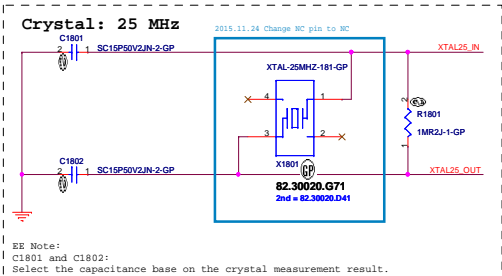
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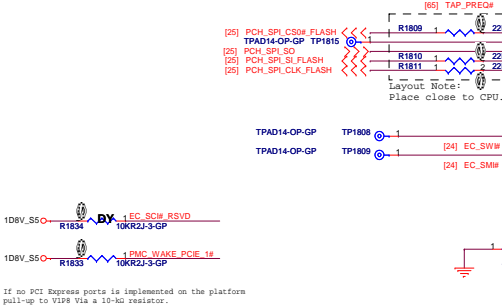
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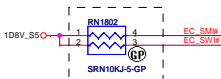
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```
(CRB#509728)
Layout Note:
1. PLACE R1806,R1813,R1814 WITHIN 1.1" FROM SOC PIN
2. PLACE R1815 WITHIN 0.25" FROM XDP PIN
```

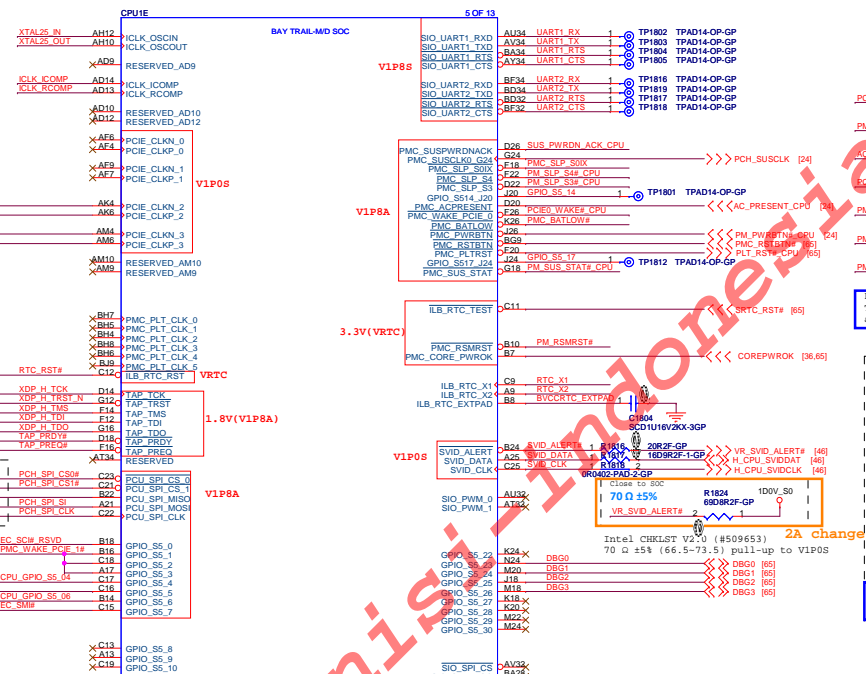
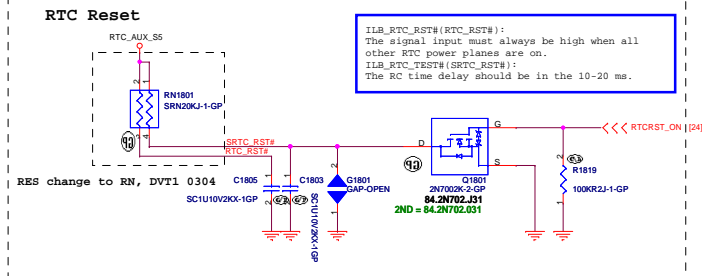
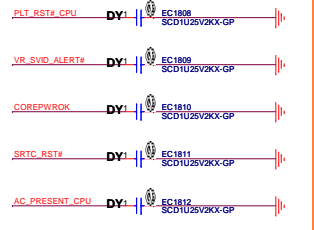


If no PCI Express ports is implemented on the platform pull-up to V1P8 Via a 10-kΩ resistor.

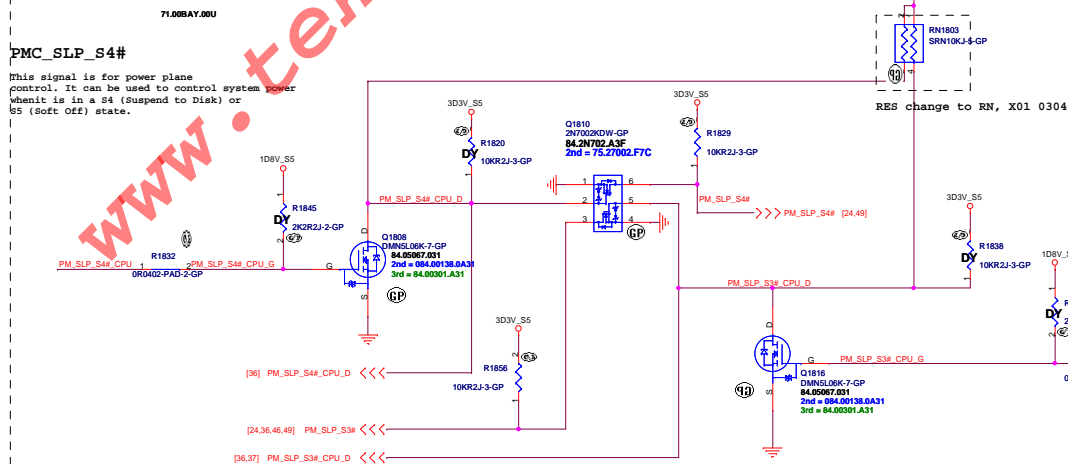


RES change to RN, DVT1 0304

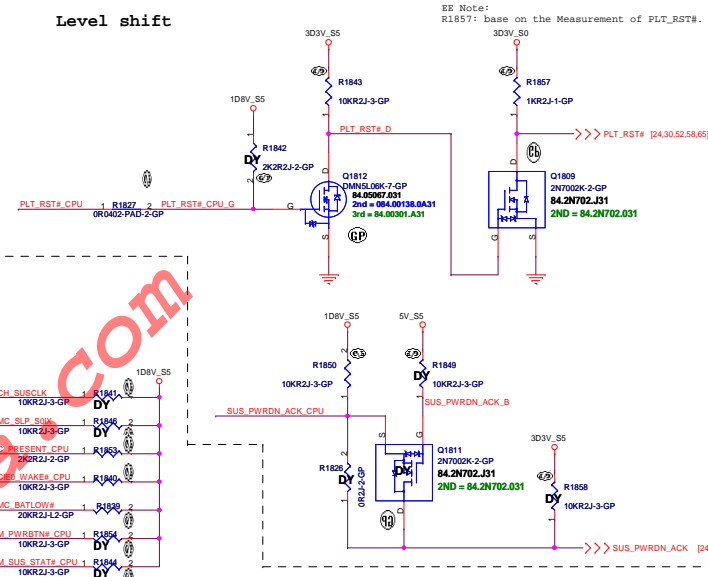
reserve the 0402 0.1u caps for EMI



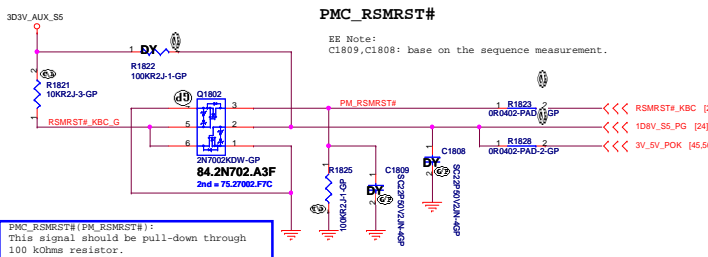
28 If the SPI interface is not implemented this signal can be left unconnected.



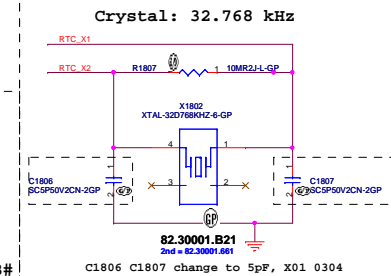
Level shift



PM_PWRBTN#_CPU (PMC_PWRBTN#):
This signal has an internal pull-up resistor
and has an internal ~16 ms de-bounce on the input.



PMC_RSMRST#(PM_RSMRST#):
This signal should be pull-down through
100 kOhms resistor.



PMC_SLP_S3#

This signal is for power plane control. It can be used to control system power when it is in a S3 (Suspend to RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.


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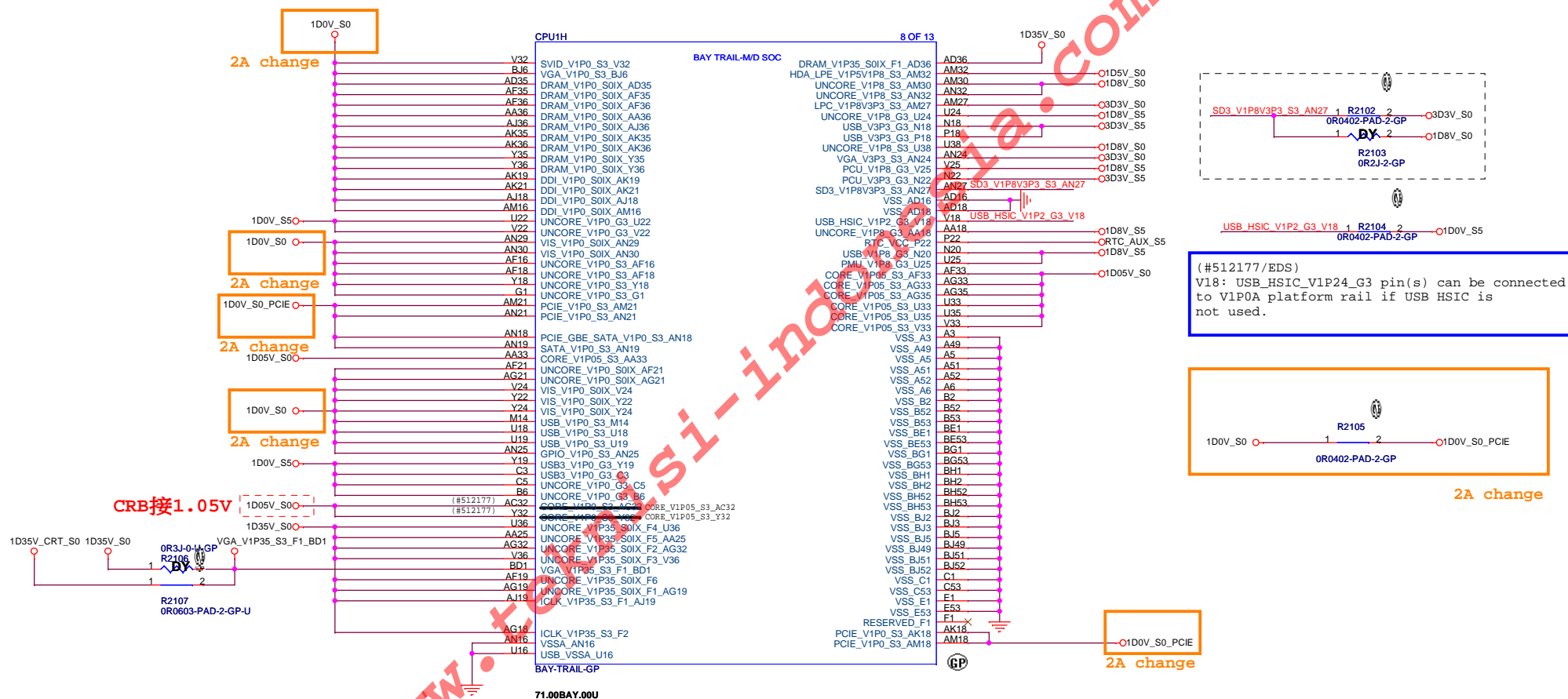
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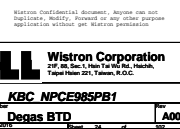
Main Func = PCH

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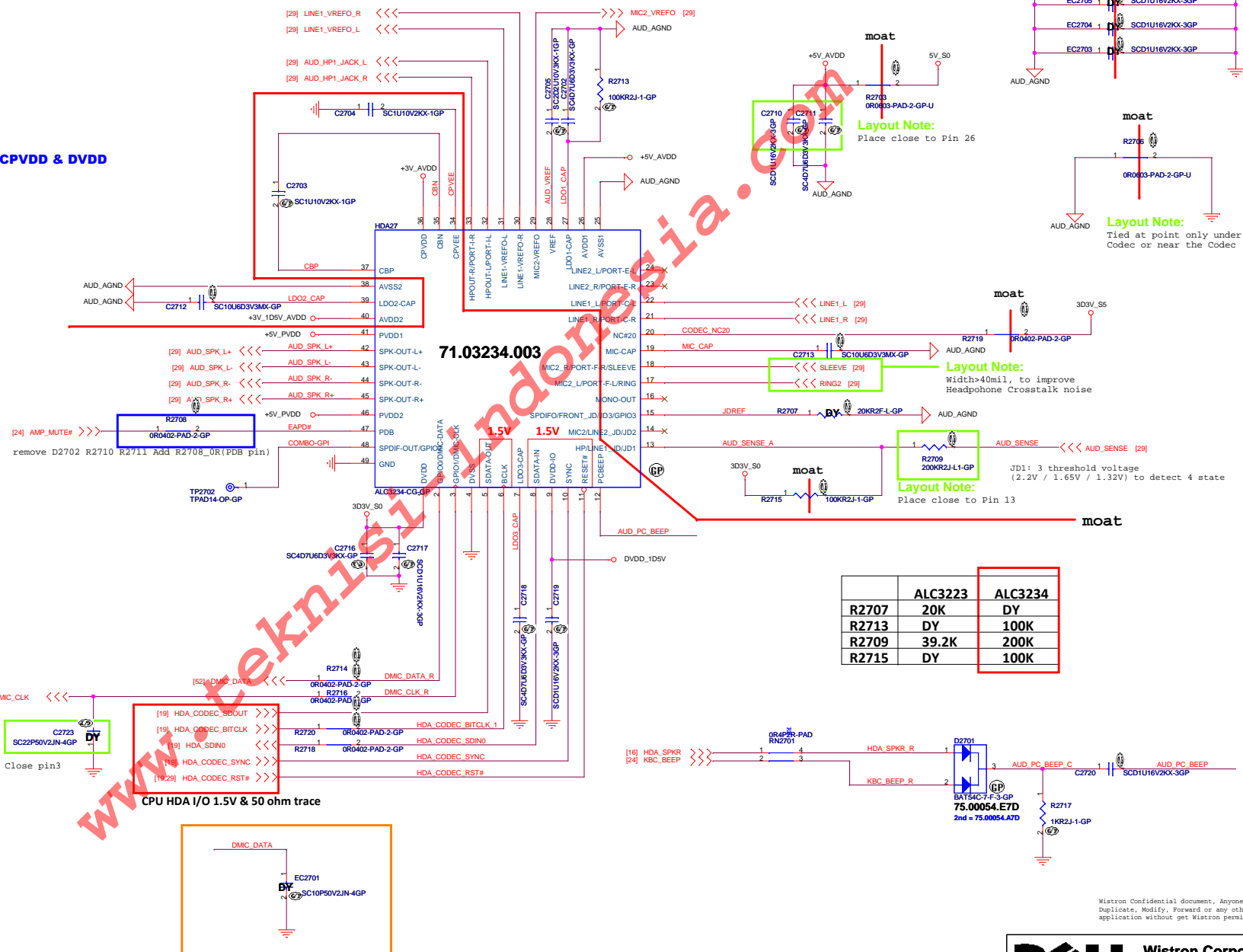
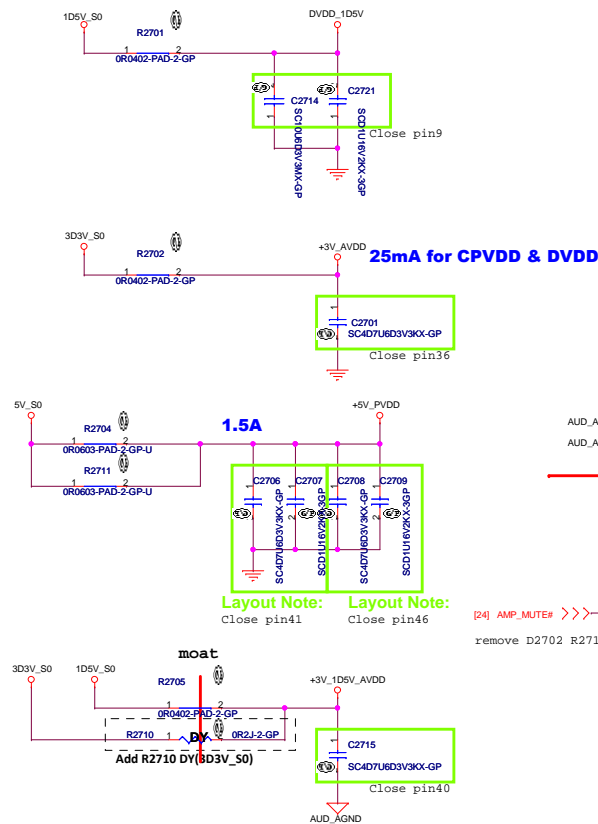
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Size A4	Document Number Degas BTD		Rev A00
Date: Monday, May 16, 2016		Sheet 23 of	102



Main Func = Audio




	ALC3223	ALC3234
R2707	20K	DY
R2713	DY	100K
R2709	39.2K	200K
R2715	DY	100K

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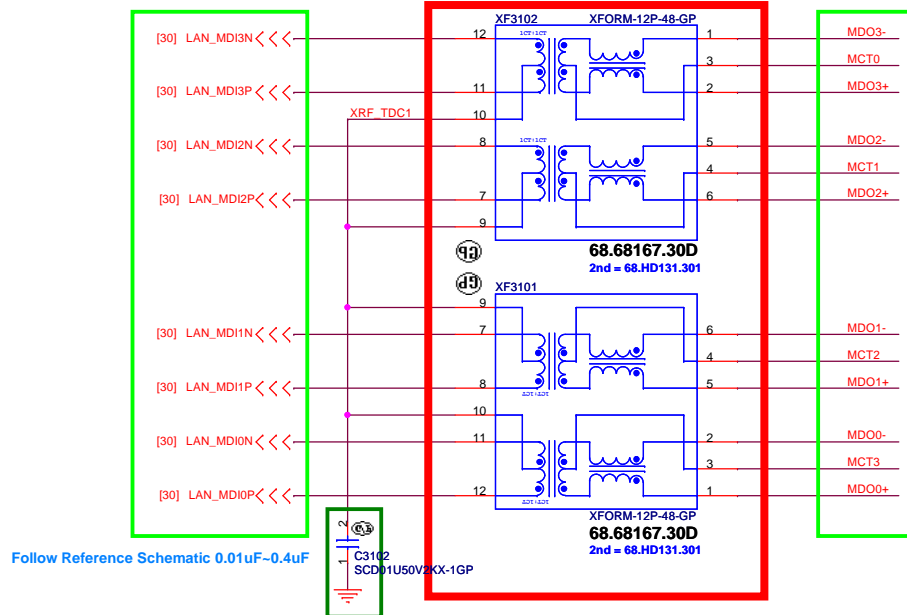
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Title (Reserved)			
Size A4	Document Number Degas BTD		Rev A00
Date: Monday, May 16, 2016		Sheet 28 of	102

Main Func = LAN

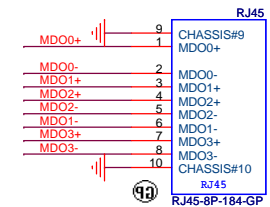
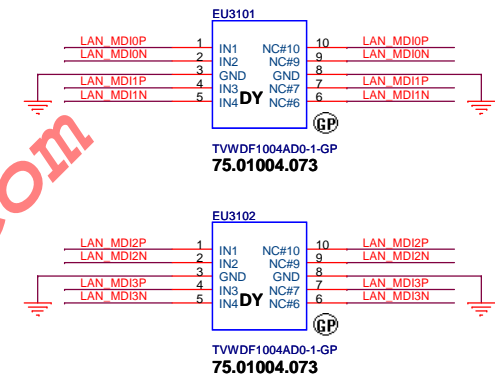
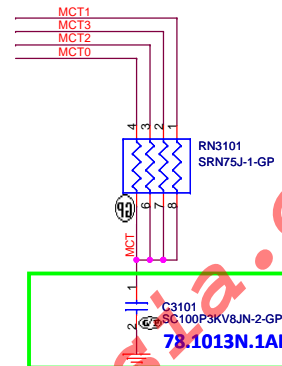
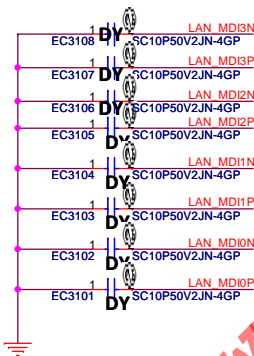
LAN Transformer (10/100/1000M)

Change to 68.68167.30B

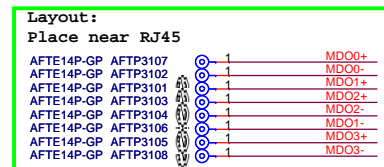


Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.



022.10001.0C41
2nd = 022.10001.0D41




Main Func = Card Reader

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Title CardReader RTL5170			
Size A4	Document Number Degas BTD		Rev A00
Date: Monday, May 16, 2016		Sheet 32 of	102

Main Func = Card Reader

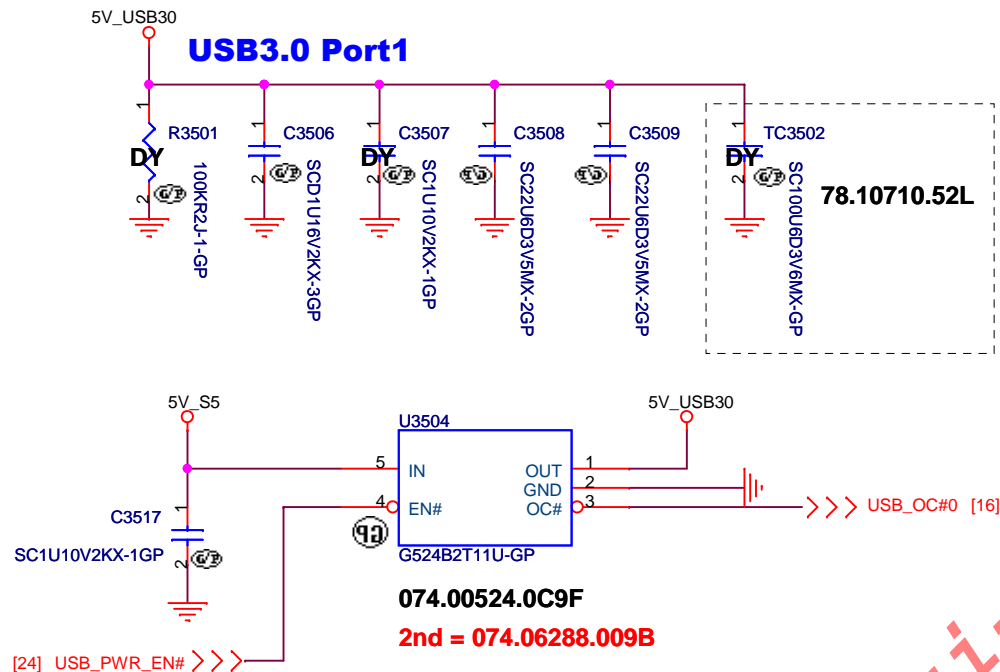
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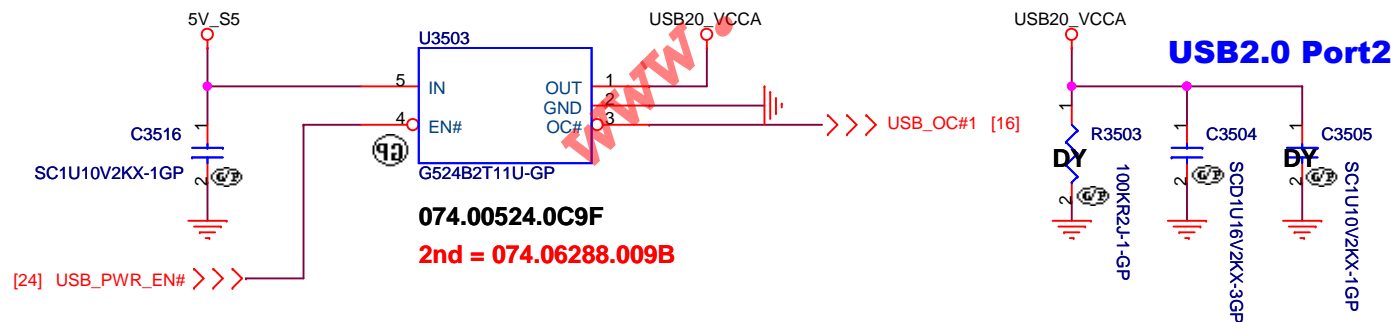
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Title Card Reader CONN			
Size A4	Document Number Degas BTD		Rev A00
Date: Monday, May 16, 2016		Sheet 33 of	102

Main Func = USB3.0



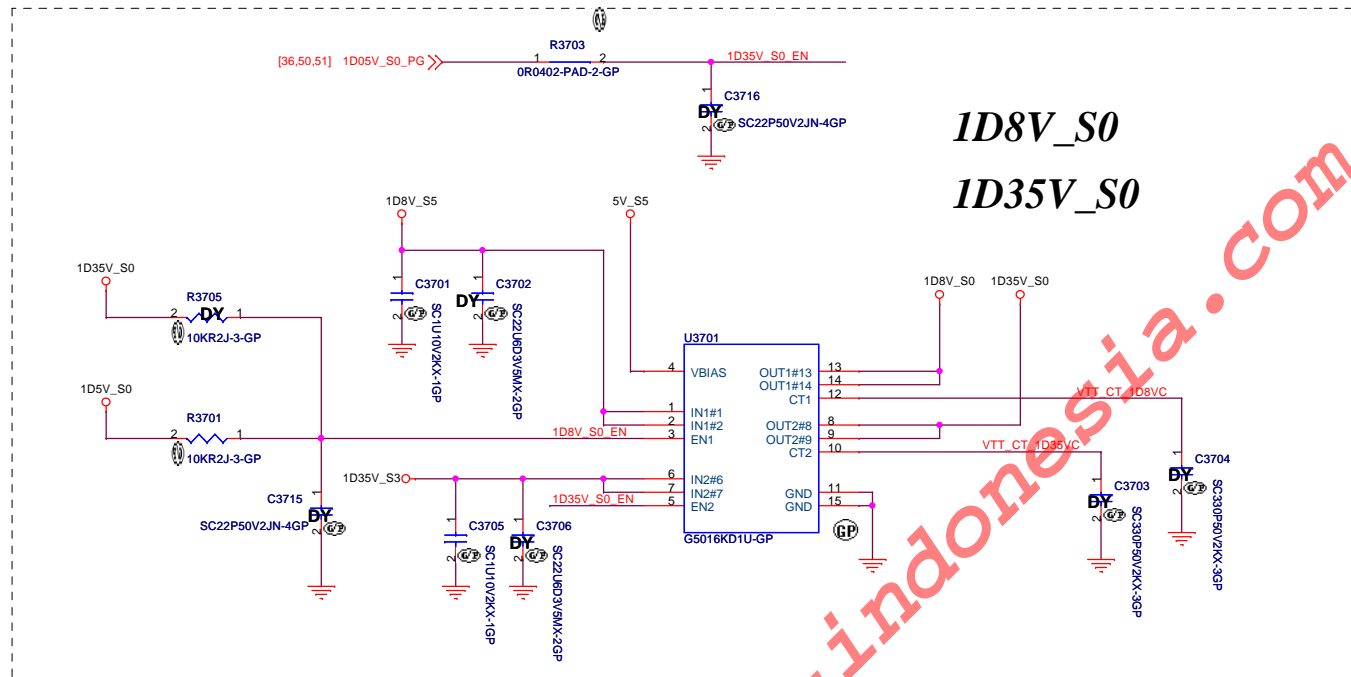
Main Func = USB2.0



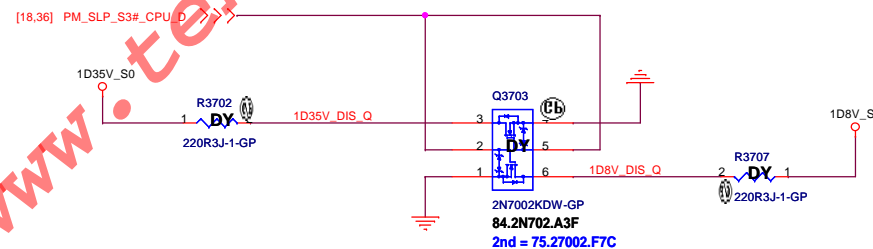
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Title		
USBPowerSW		
Size	Document Number	Rev
A4	Degas BTD	A00
Date:	Monday, May 16, 2016	Sheet 35 of 102

Main Func = Power Plane & Sequence



Discharge circuit



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Title			Run Power		
Size	Document Number		Degas BTS		Rev
A3					A00
Date:	Monday, May 16, 2016		Sheet	37	of 102

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Title (Reserved)			
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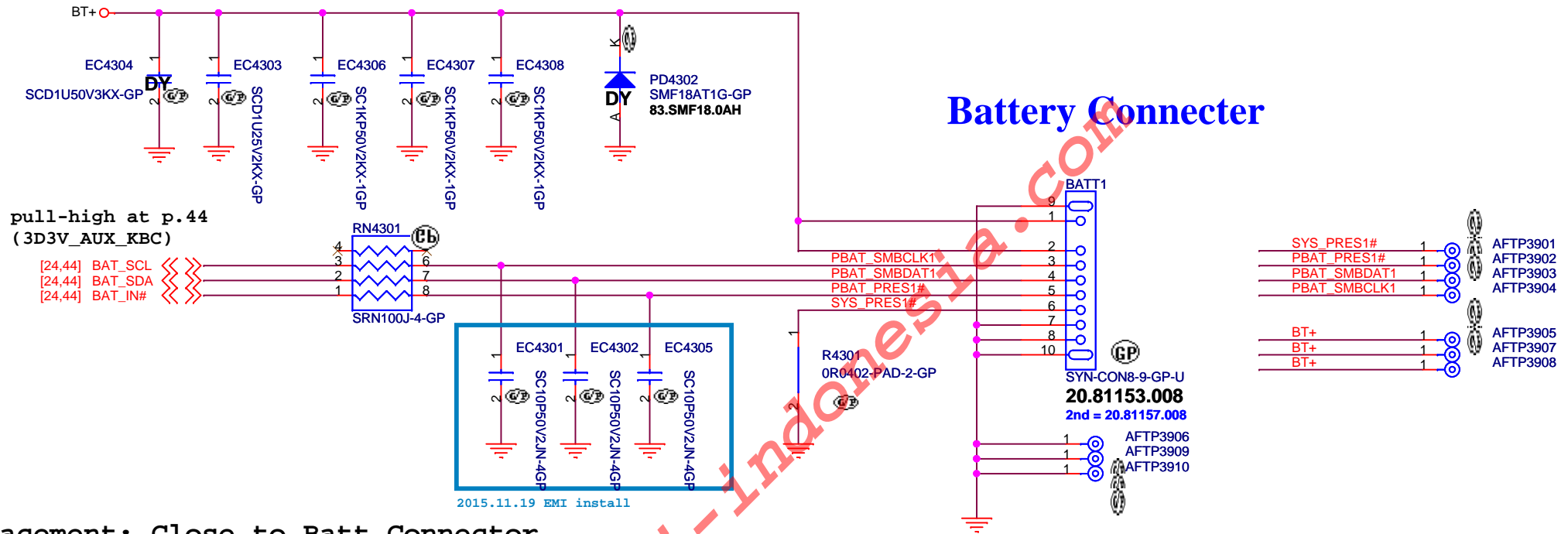
Main Func = ADT Input

Layout Note:
PSID Layout width > 25mil

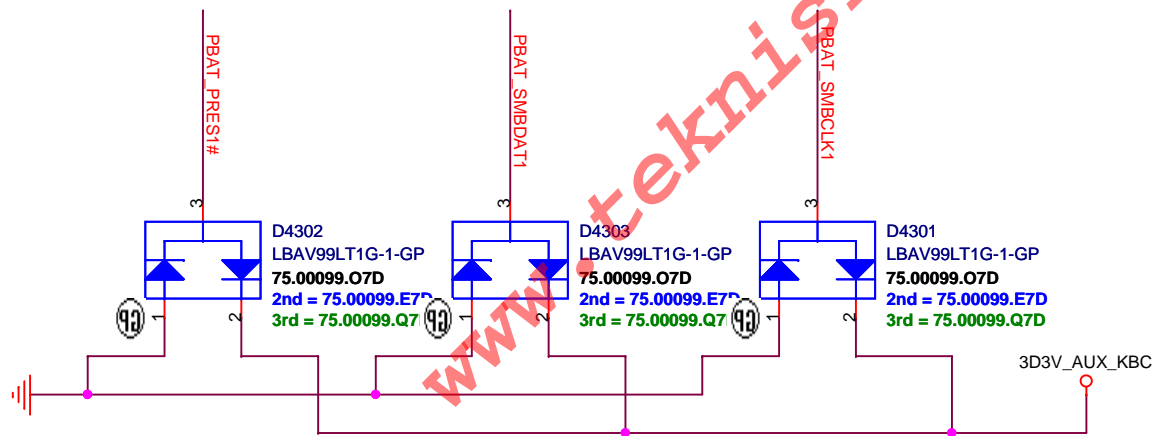
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

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Title _____			
Size A3		Document Number _____	
Date: Monday, May 16, 2016		Sheet 42 of 102	
_____		_____	

Main Func = M-BAT Input



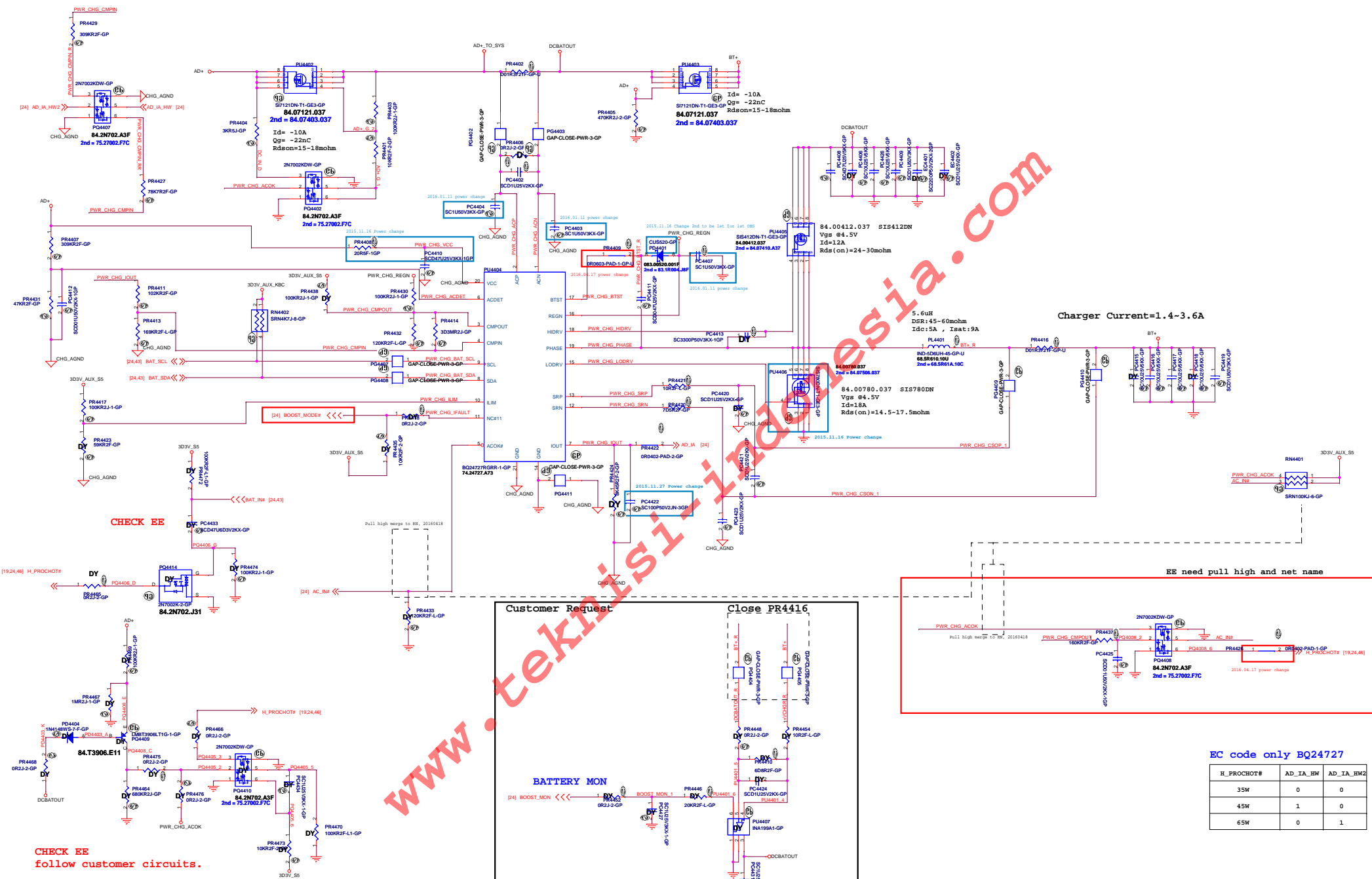
Placement: Close to Batt Connector



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Title BATT CONN			
Size A4	Document Number Degas LTD		Rev A00
Date: Monday, May 16, 2016	Sheet 43 of 102		

Main Func = Charger

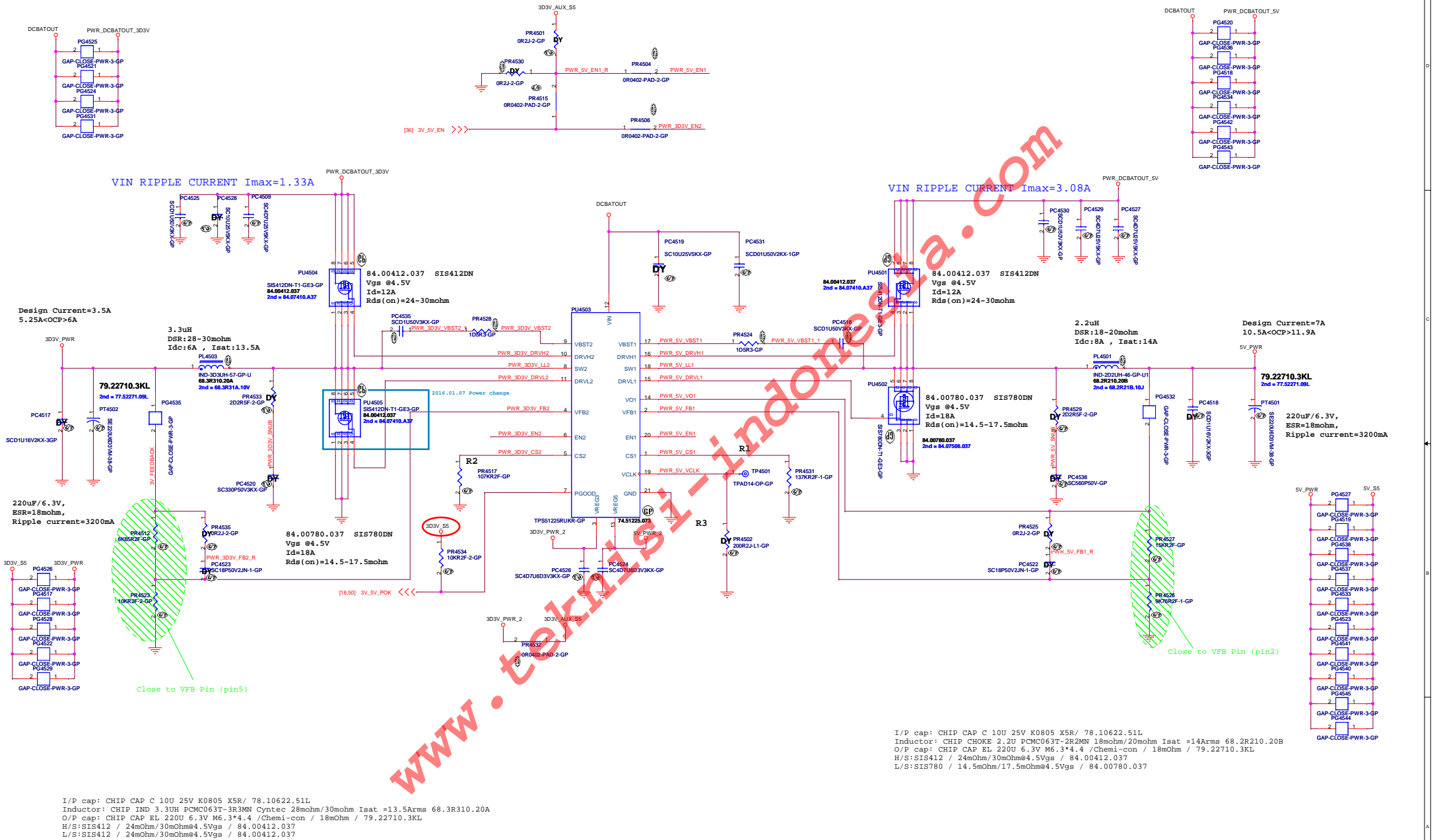


EC code only BQ24727

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
35W	0	0
45W	1	0
65W	0	1

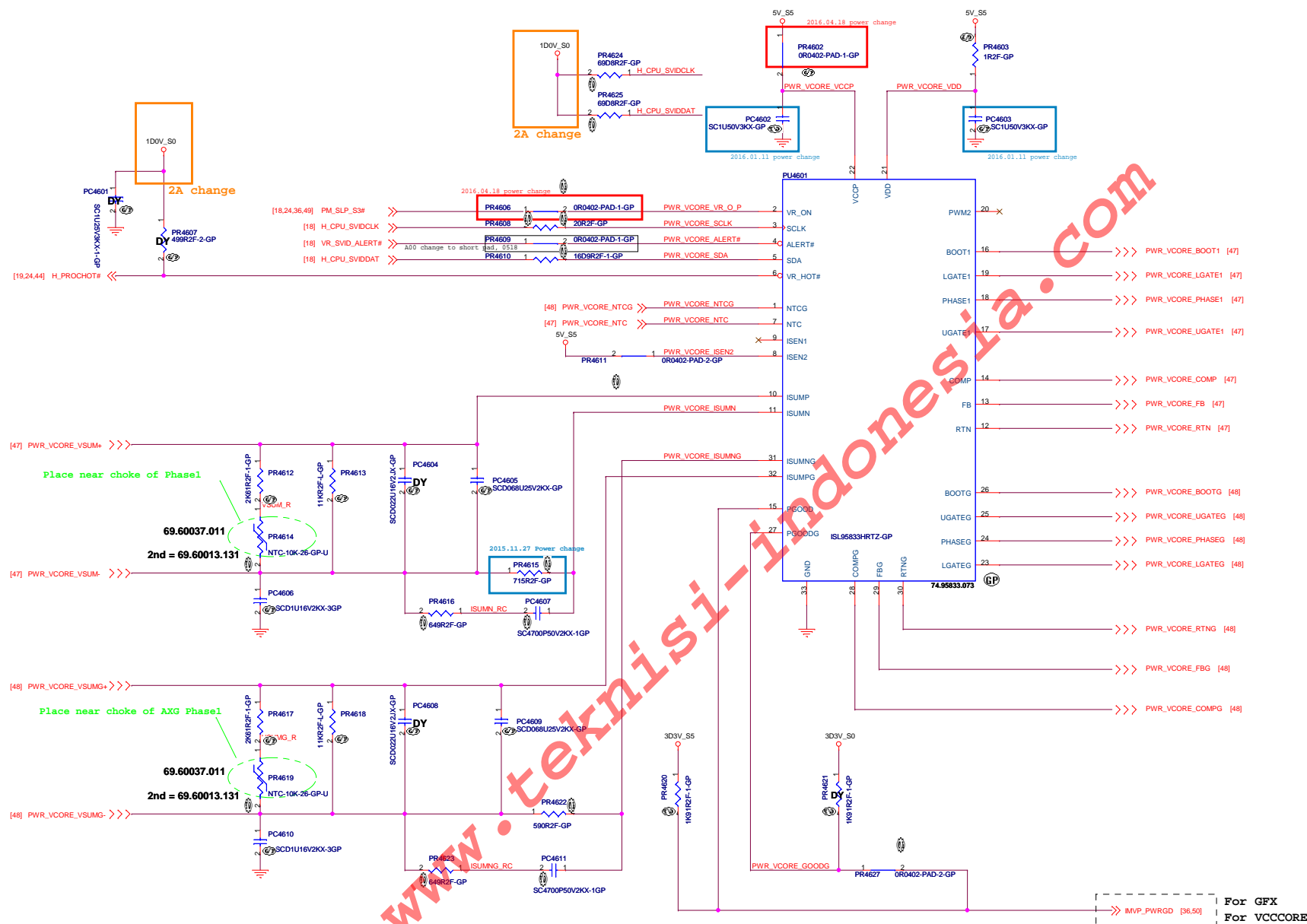
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Main Func = 3D3V_5V



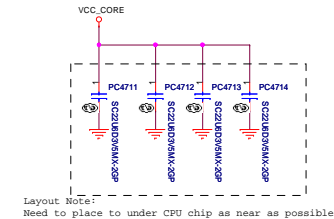
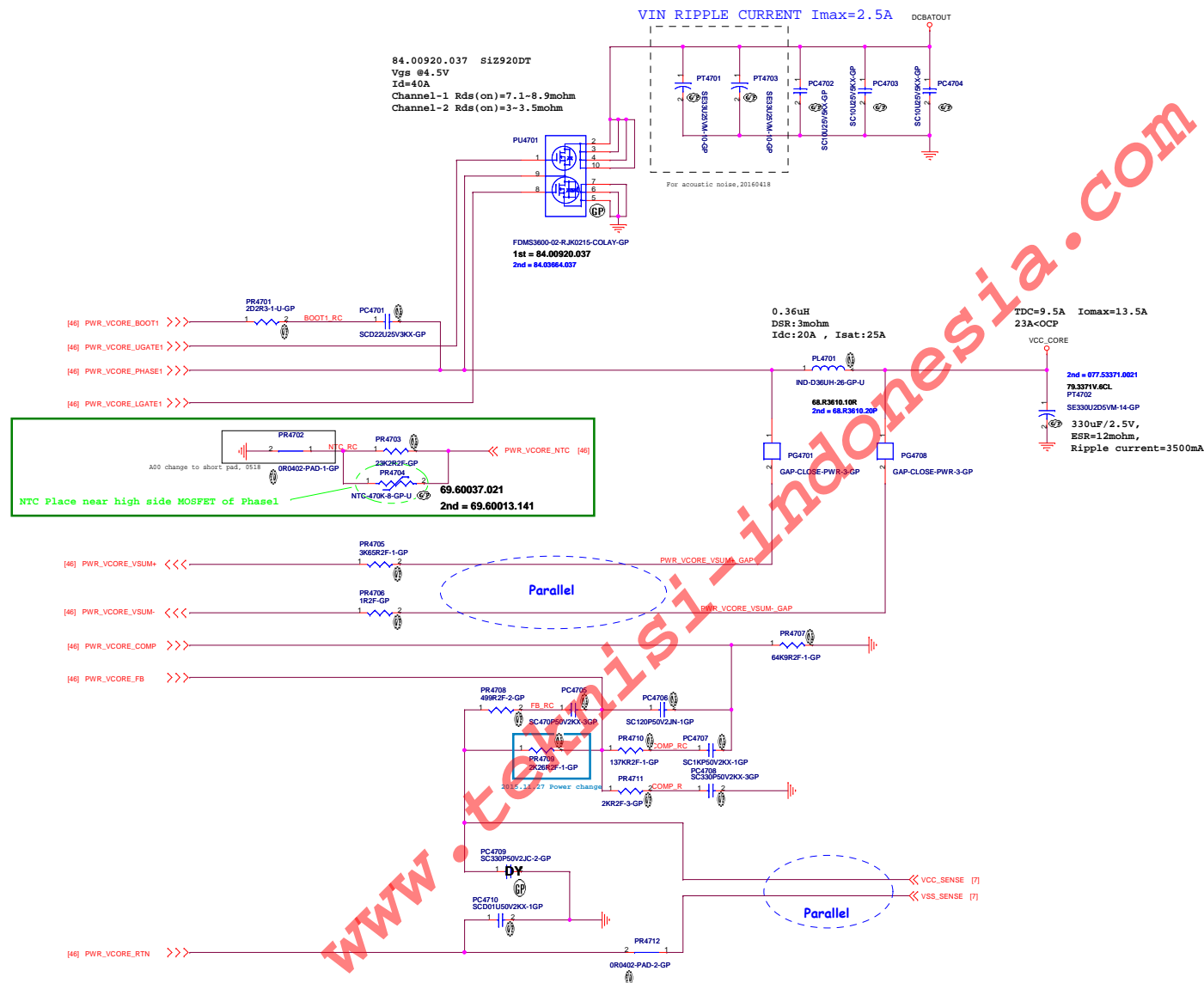
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Main Func = CPU_CORE



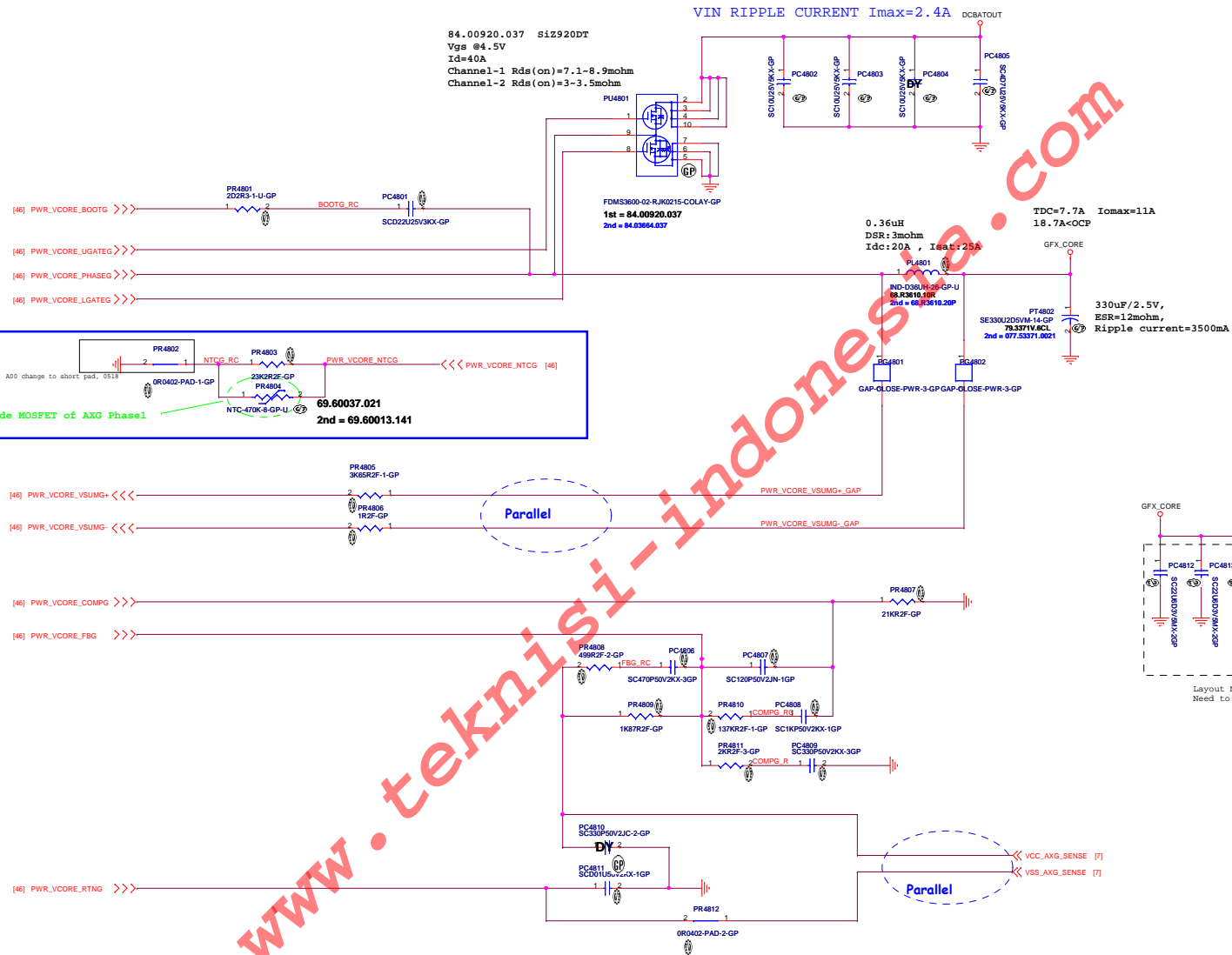
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Main Func = CPU_CORE



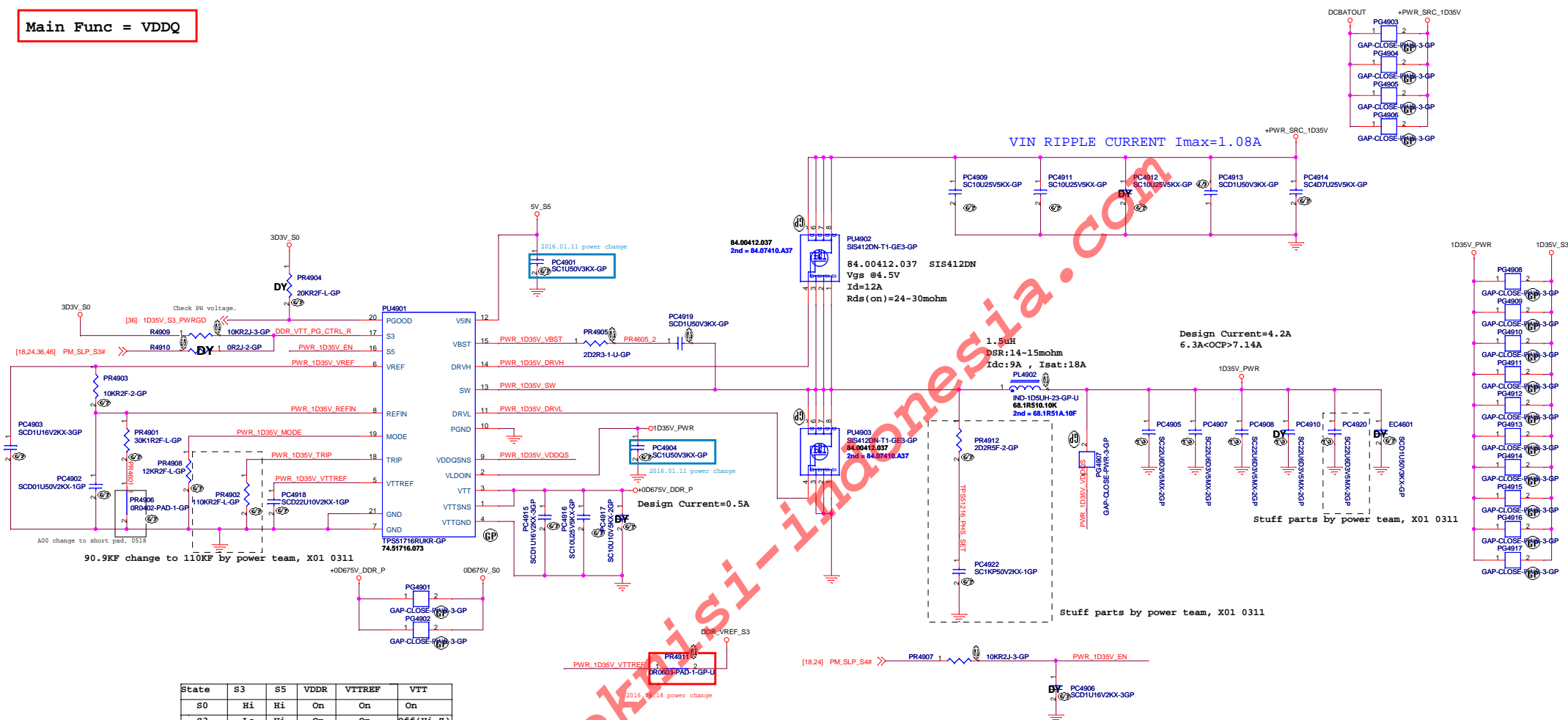
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Main Func = CPU_CORE



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Main Func = VDDQ



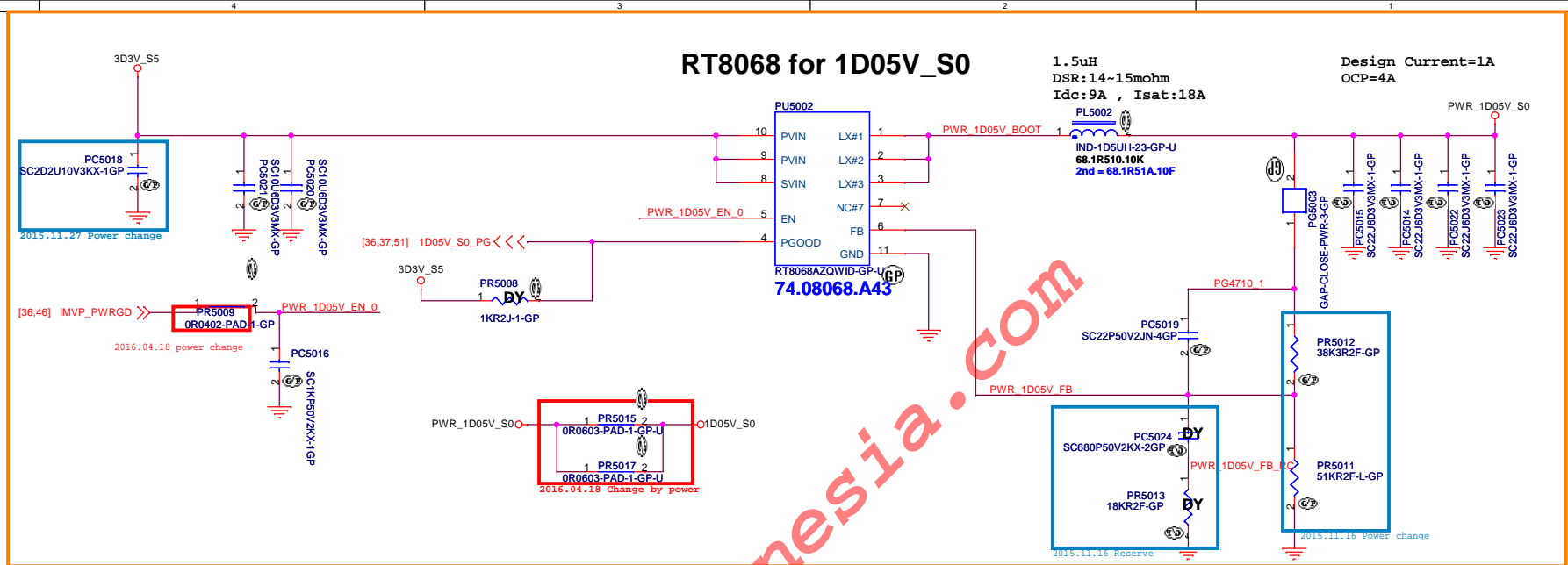
State	S3	S5	VDDR	VITREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

TPS51716 MODE

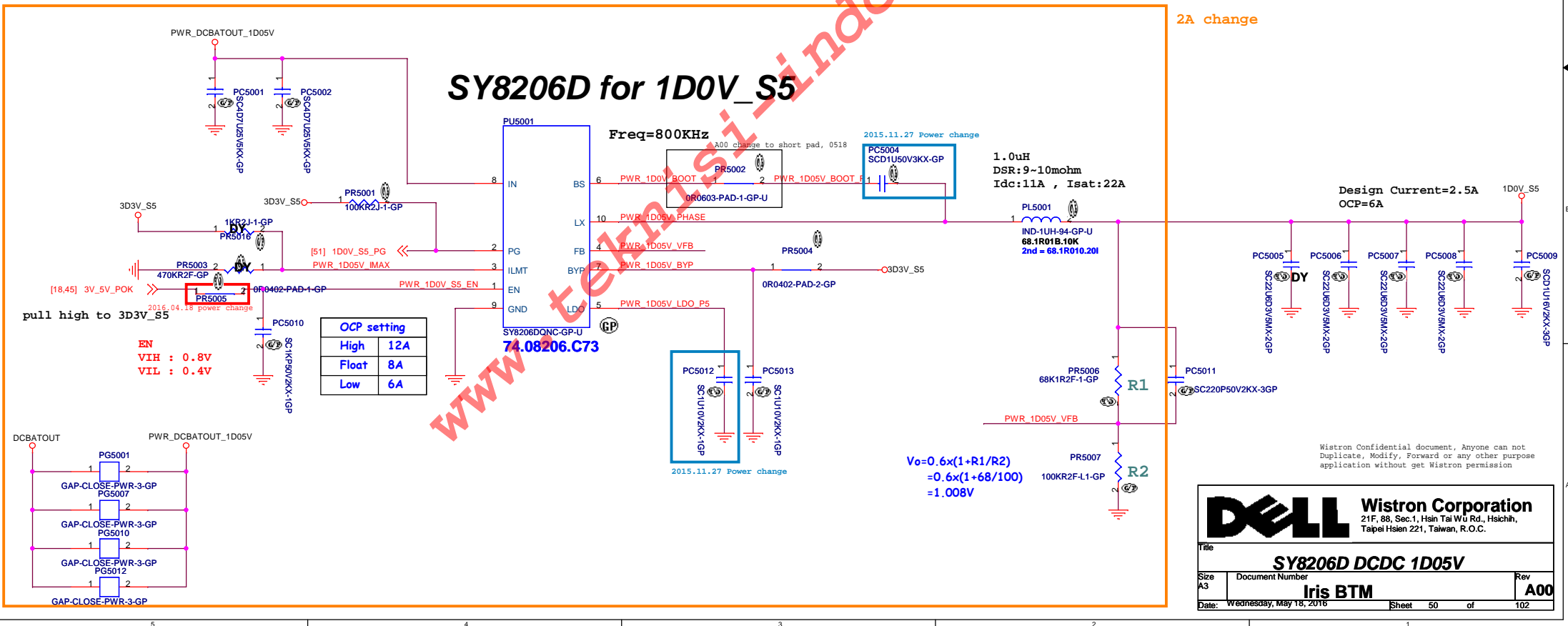
PR4908	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.5U PCMC063T-1R5MN 14-15mohm Isat =18Arms 68.1R510.10K
H/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V
L/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V

Main Func = 1D05V



2A change



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SY8206D DCDC 1D05V

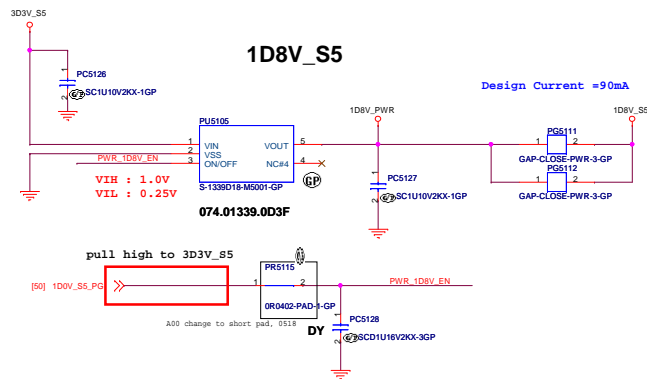
Size	Document Number
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A3 **Iris BTM**

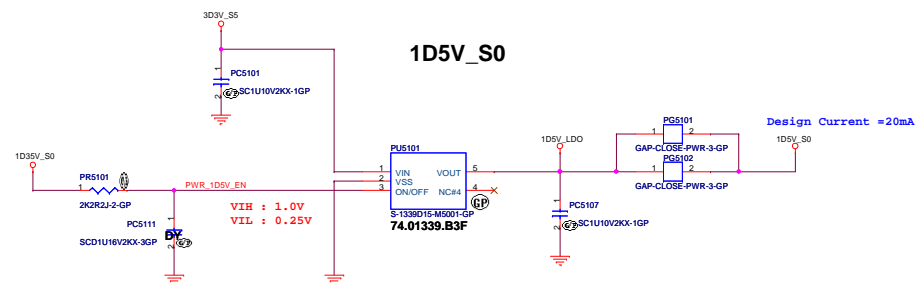
Date: Wednesday, May 18, 2016

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Main Func = 1D8V

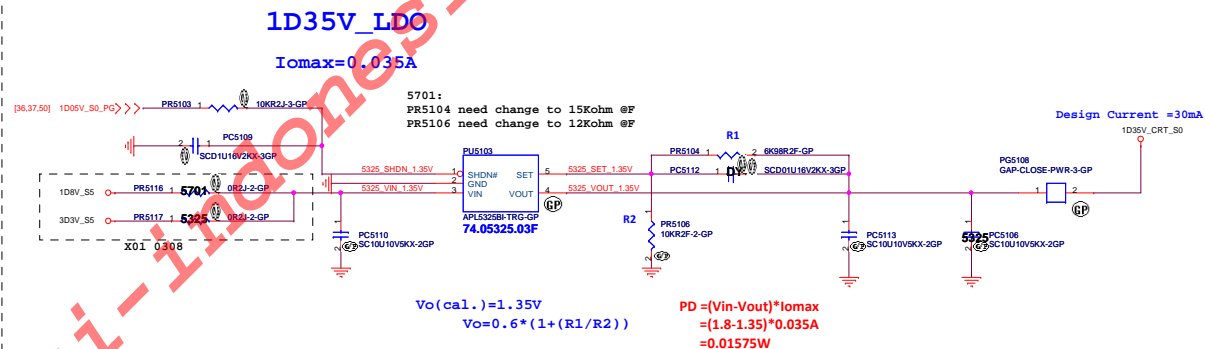


Main Func = 1D5V

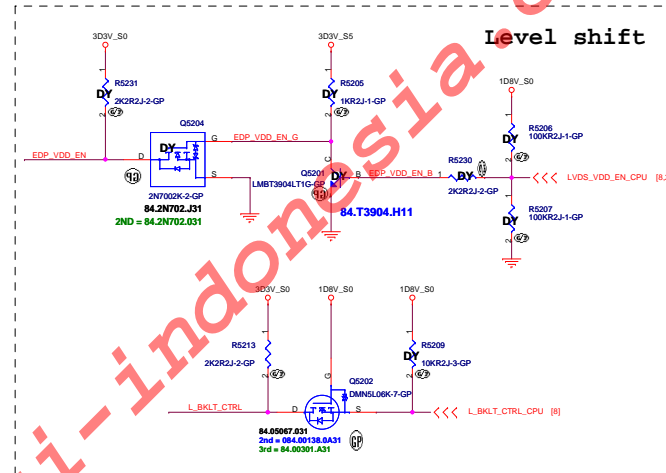
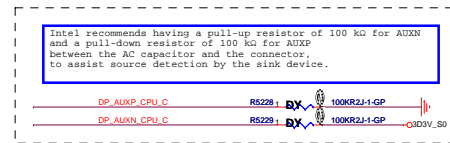
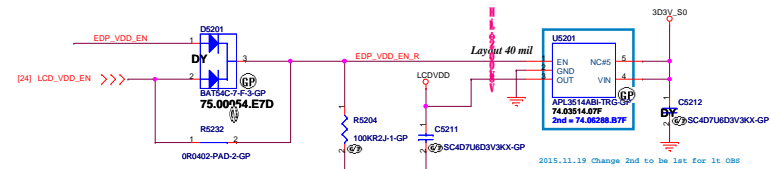
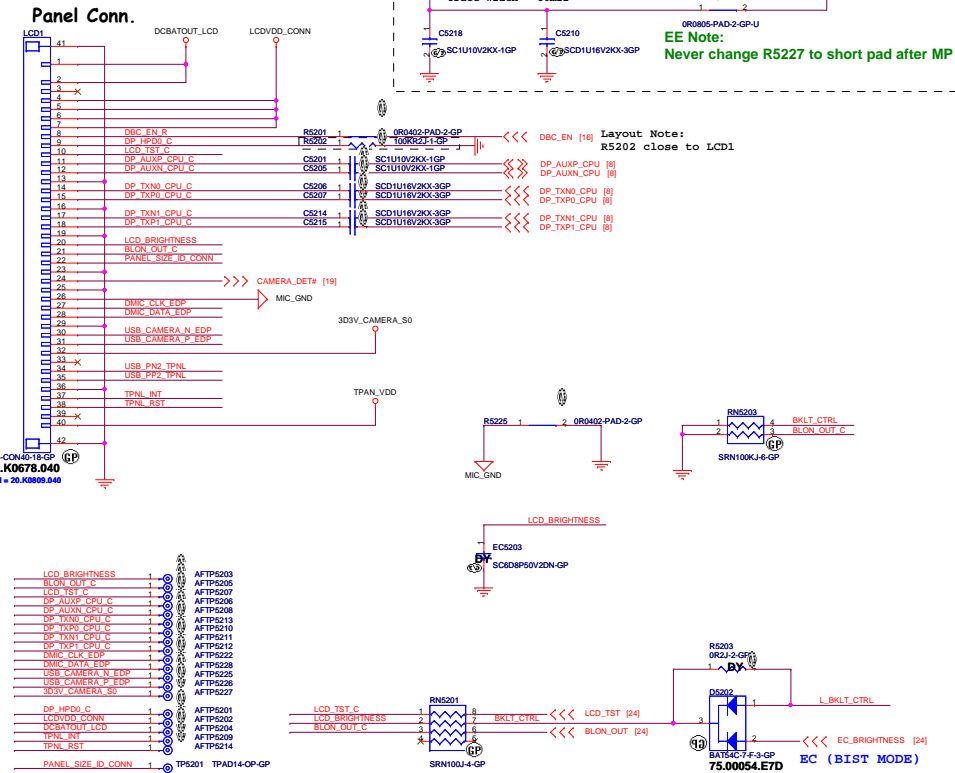


Main Func = 1D0V

```
Main Func = 1D35V
```

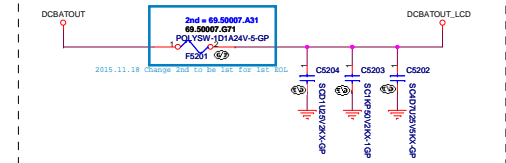


Main Func = LCD

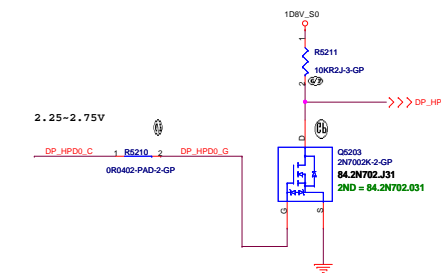


INVERTER POWER

EE Note:
Never change R5208 to short pad after MP



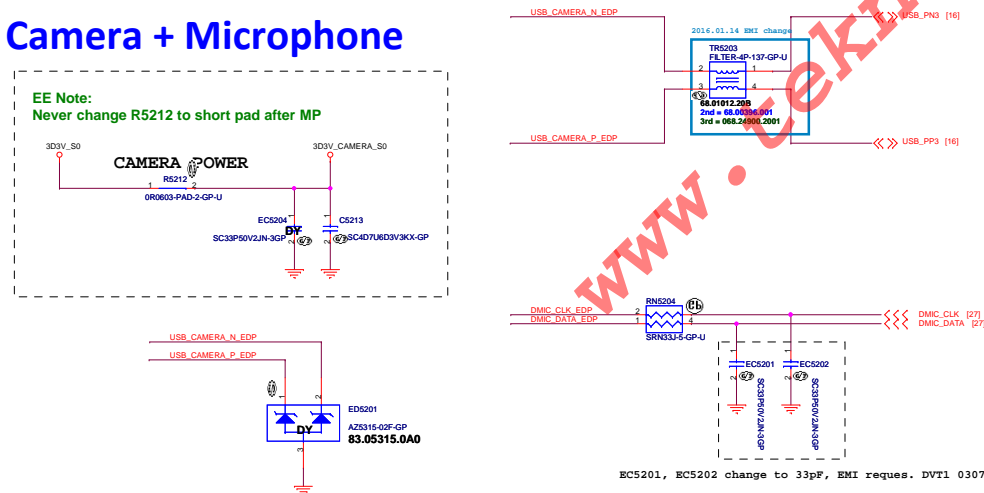
EE Note:
Need to check LCD Panel spec for
HPD voltage level.
Layout Note:
Place PL resistor of DP_HPD0_C close to LCD1.



Main Func = Camera + DMIC

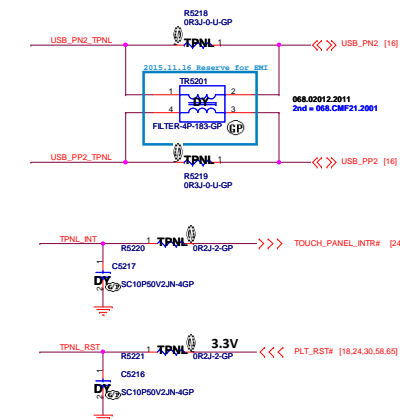
Camera + Microphone

EE Note:
Never change R5212 to short pad after MP

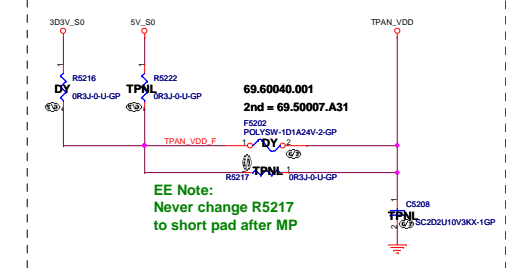


Main Func = TS

Touch Screen

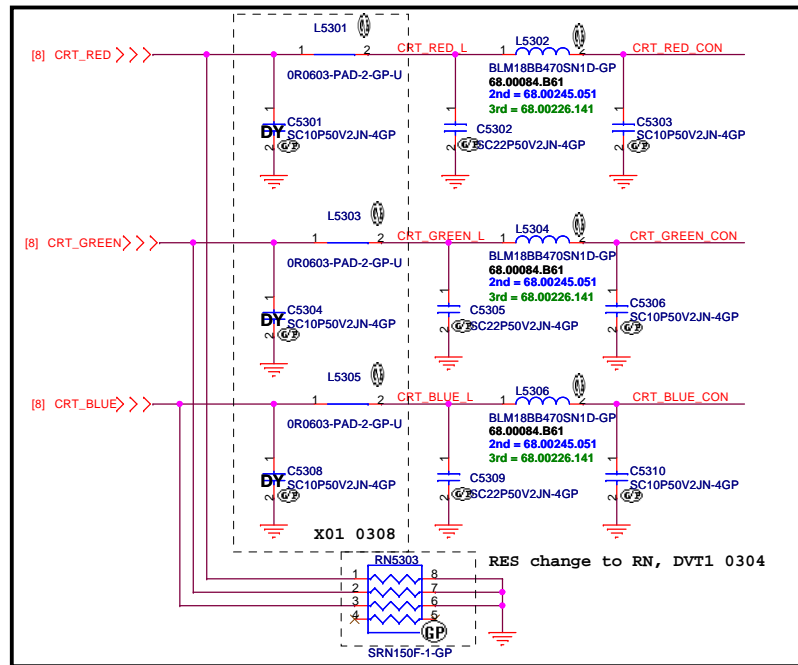


TOUCH PANEL POWER

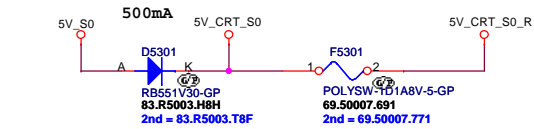
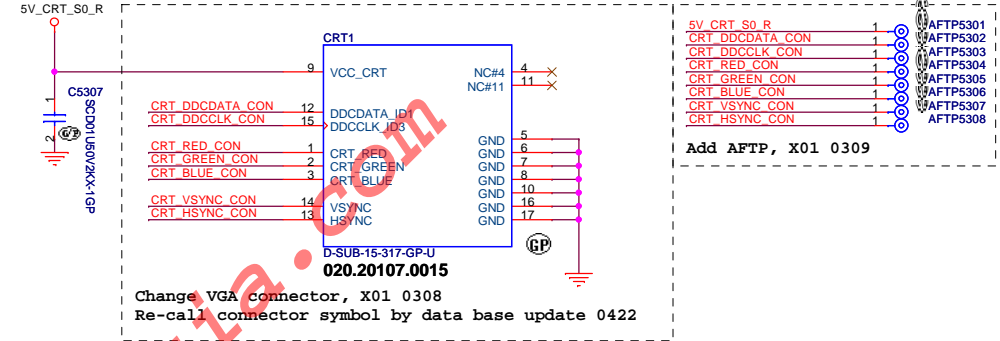
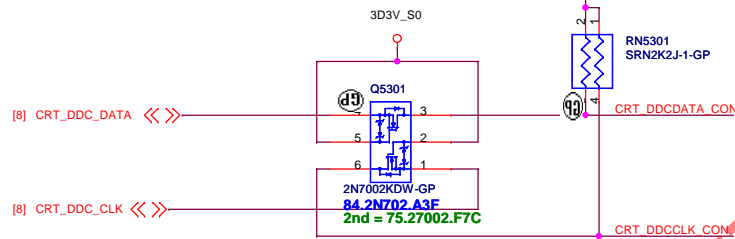


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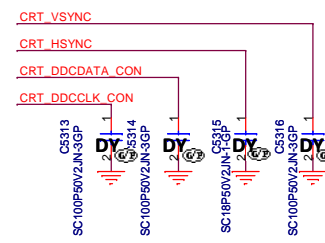
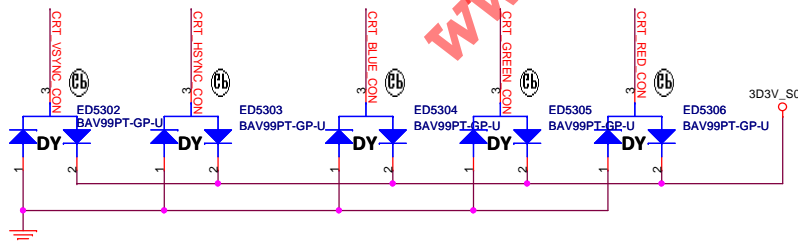
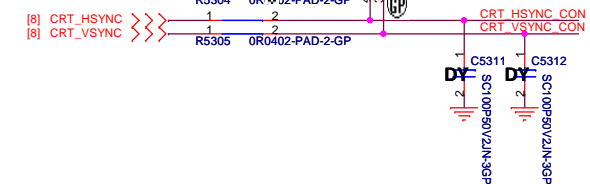
Close to CRT1



CRT DDCDATA & DDCCLK level shift



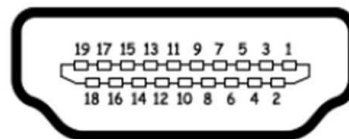
CRT Hsync & Vsync



Main Func = HDMI

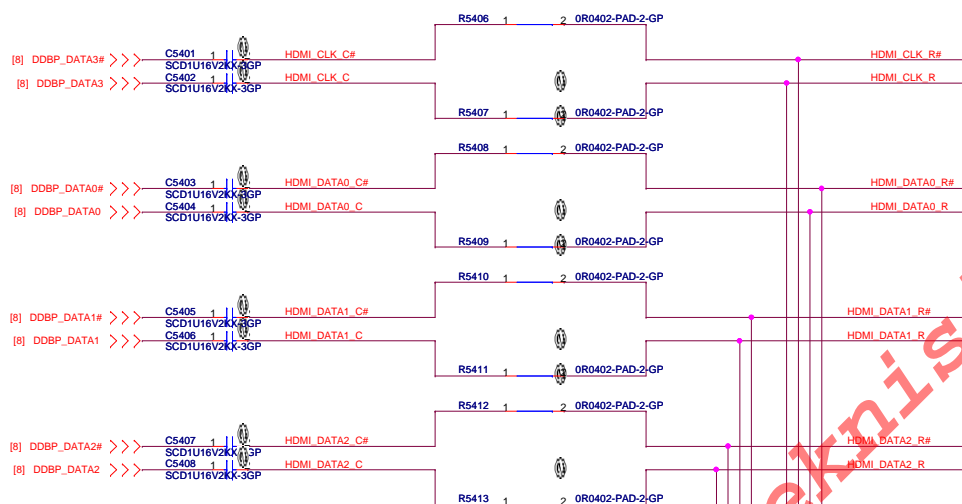
HDMI Level Shifter & Connector

Stuff part, EMI request. DVT1 0307

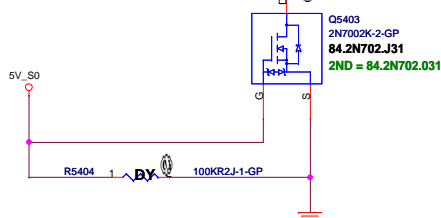


Reserve 150 ohm bridge resistance on the HDMI trace as circle for EMI.

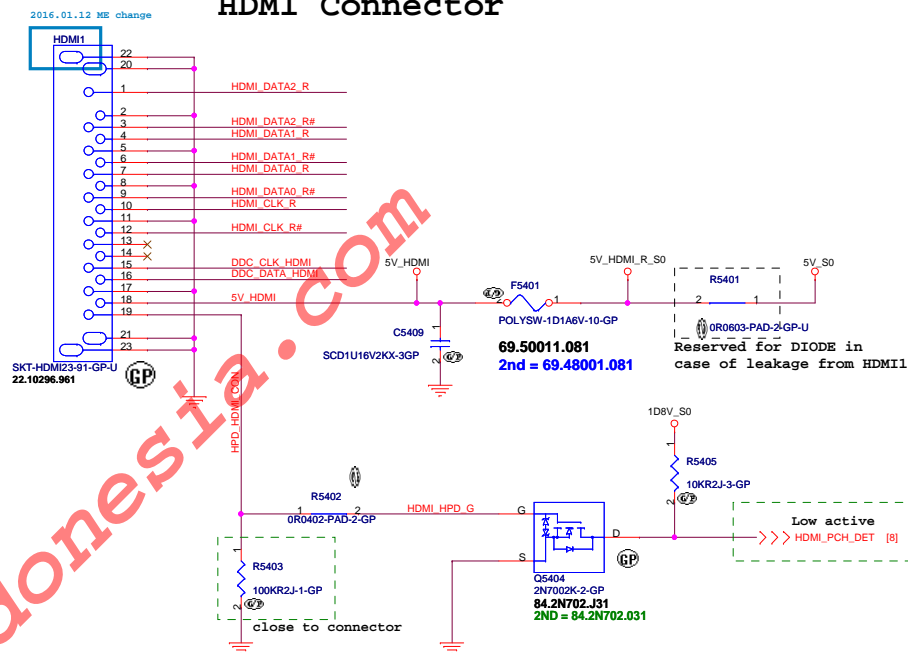
Pin#	Signal	Pin#	Signal
1	TMDS data 2+	11	TMDS clock shield
2	TMDS data 2 shield	12	TMDS clock-
3	TMDS data 2-	13	CEC
4	TMDS data 1+	14	No connected
5	TMDS data 1 shield	15	DDC clock
6	TMDS data 1-	16	DDC data
7	TMDS data 0+	17	Ground
8	TMDS data 0 shield	18	+5V power
9	TMDS data 0-	19	Hot plug detect
10	TMDS clock+		



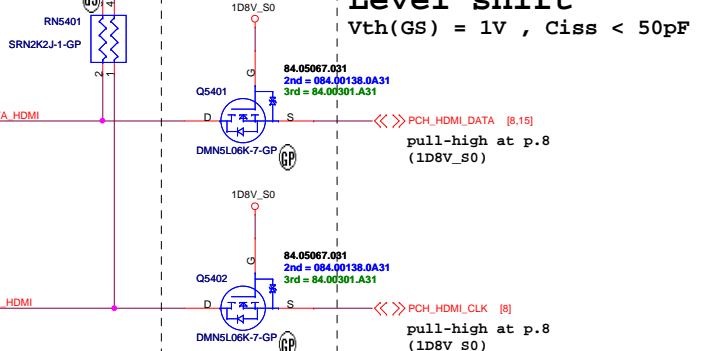
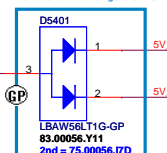
PDG(#512238): 620 Ω \pm 5%



HDMI Connector



2016.01.12 change for OBS




Level shift
 $V_{th}(GS) = 1V$, $C_{iss} < 50pF$

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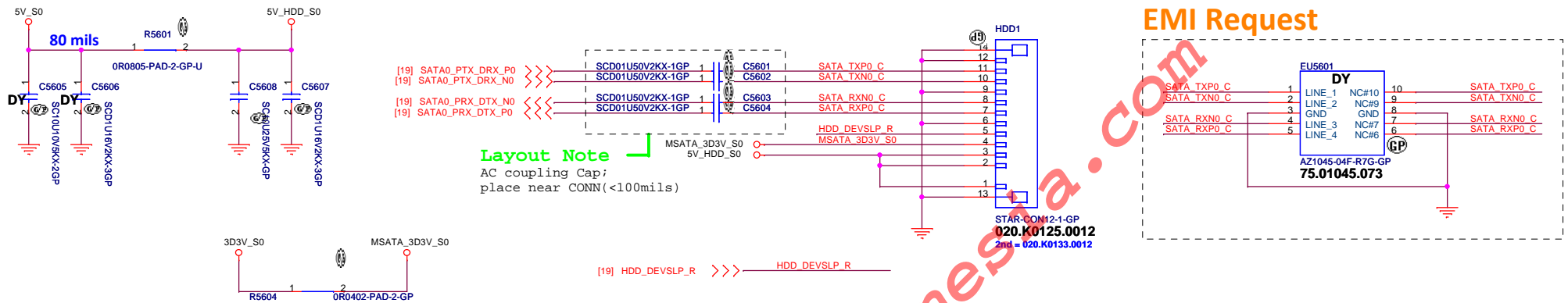
Blanking

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Title			
<i>Reserved</i>			
Size A4	Document Number		Rev A00
Date: Monday, May 16, 2016		Sheet 55 of	102

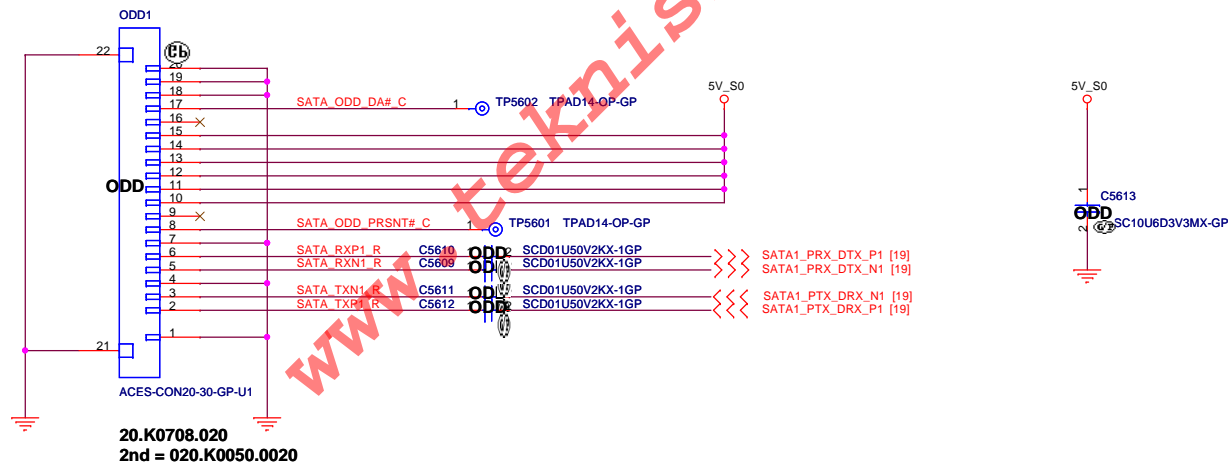
Main Func = HDD

SATA HDD Connector



Main Func = ODD

ODD Connector



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Title			HDD/ODD	
Size	Document Number	Rev		
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Title (Reserved)			
Size A4	Document Number Iris BTM		Rev A00
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Main Func = WWAN/mSATA

Blanking

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Title

(Reserved)

Size
A4

Document Number
Degas BTD

Rev
A00

Date: Monday, May 16, 2016


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Main Func = mSATA

Blanking

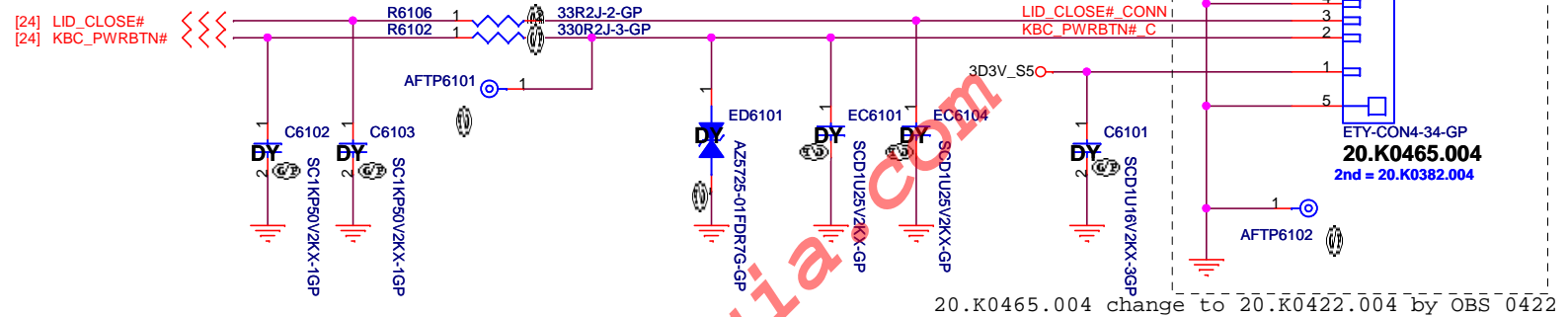
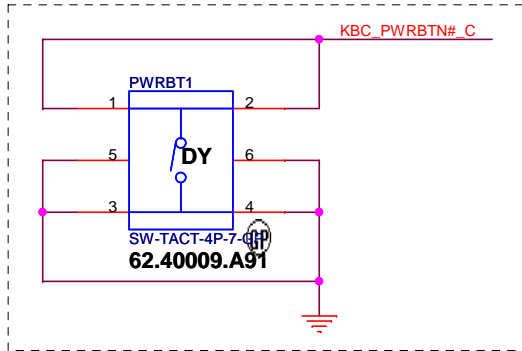
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Title (Reserved)			
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Main Func = Power BTN

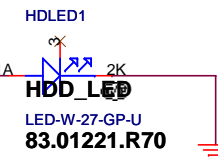
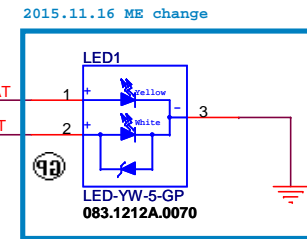
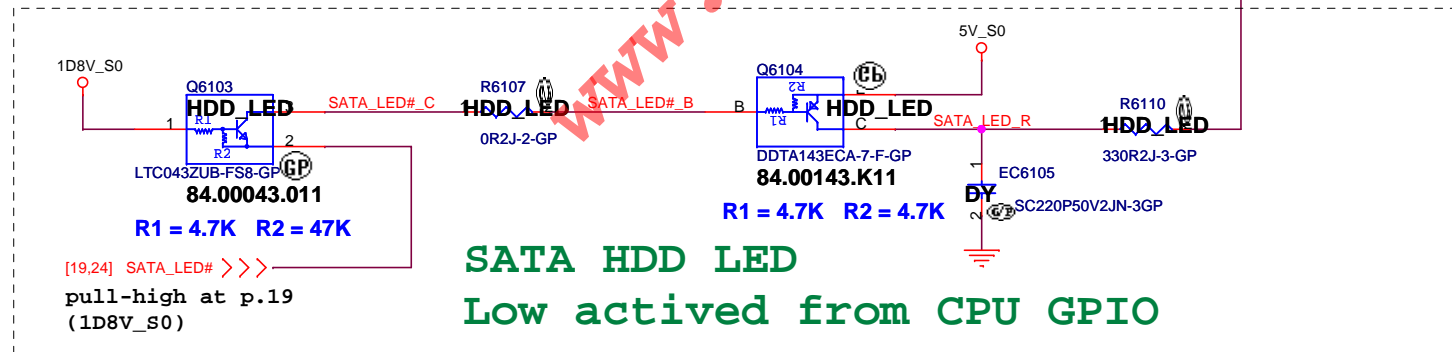
Power Button & Hall Sensor



Main Func = LED

Battery LED1
Low activated from KBC GPIO

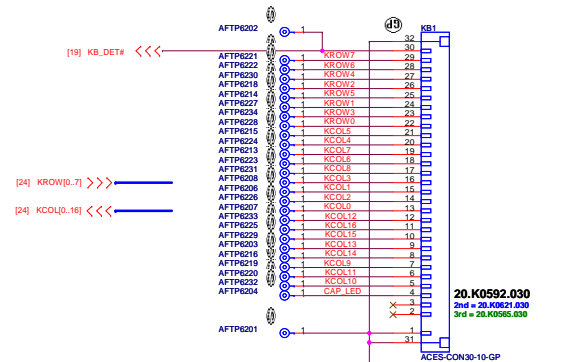
Battery LED2
Low activated from KBC GPIO



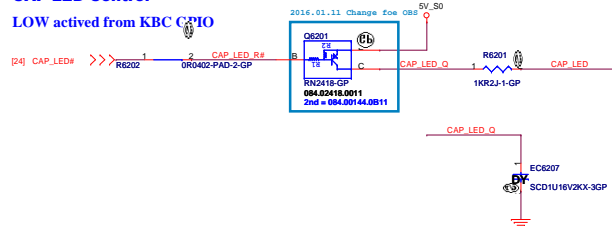
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Title LEDBard/PowerButton			
Size Custom	Document Number Degas BTD		Rev A00
Date: Monday, May 16, 2016	Sheet 61	of 102	

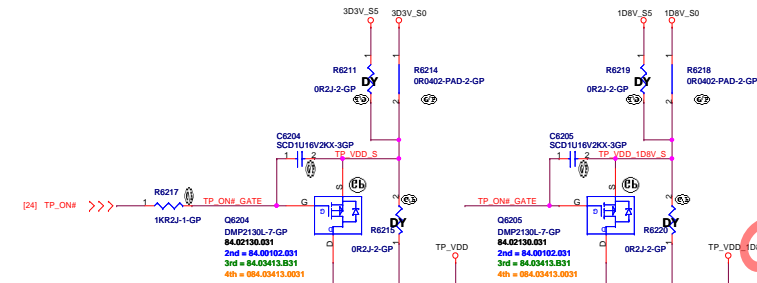
Keyboard



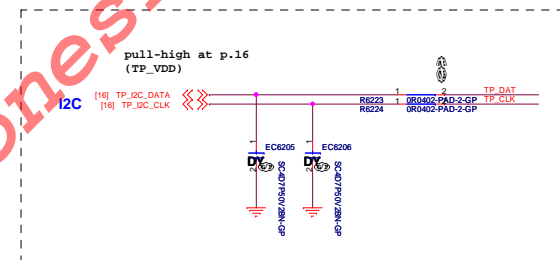
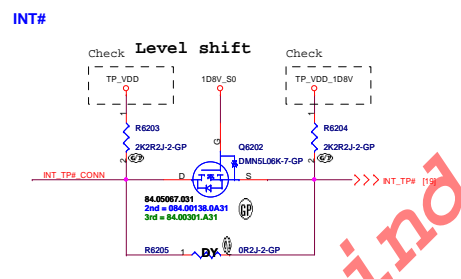
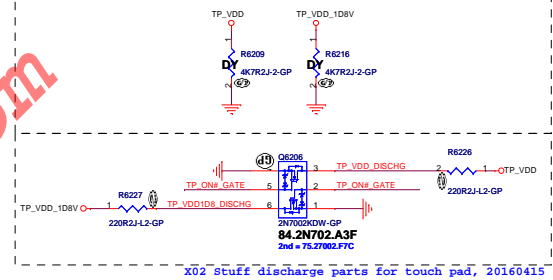
LOW actived from KBC GPIO



Touchpad Power



EE Note:
R6209,R6216,Q6206,R6226,R6227 are for Touchpad discharge.



TP_VDD

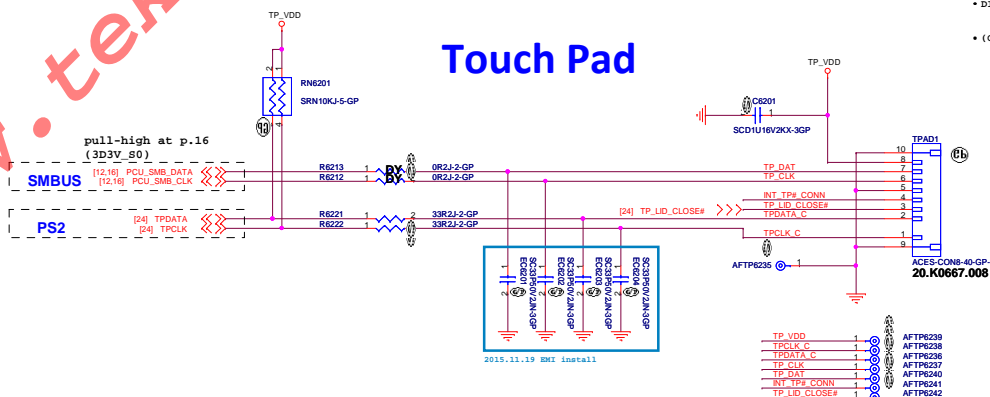
DY1

R6225

10KR2J-3-GP

TP_LID_CLOSE#

Touch Pad



```
(#514849)I2C PTP Pins
Standard I2C pins for interrupt driven I2C device:
+3.3V VDD
GND
SCL (clock)
SDA (data)
INT# (or DINT#; interrupt), also known as ATT# (attention)
-Active low

Other pins needed on I2C PTP:
-wake# - level trigger signal from PTP to Host
-Overload the INT#/ATT#/ATT# line (on the same pin)
-Only used during S3
-Active low
-Connect to either wake capable mechanism on chipset
-GPIO Pin (Suspend Well powered) for S3 platform
-Connect to EC (and route to GPIO27 or FWRST# on chipset)
-DISE (Interrupt disable)
-Active trigger signal from sensor (slave mode decoder) to PTP
-level low (active = disable any interrupt, including wake)
-(Optional) +1.8VDD
```

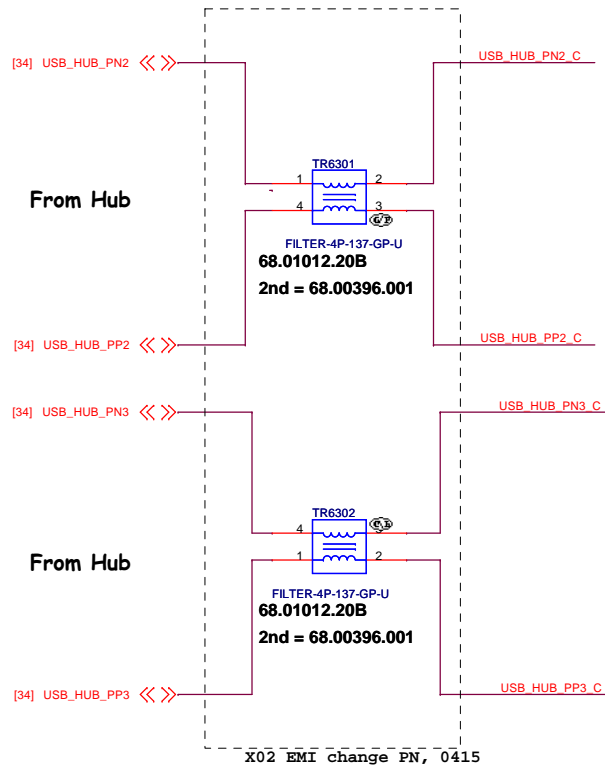
Pin No.	Pin name
1	VDD (3.3V)
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	INT#
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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Title KeyBoard/TouchPad			
Size A2	Document Number Degas BTD	Rev A00	
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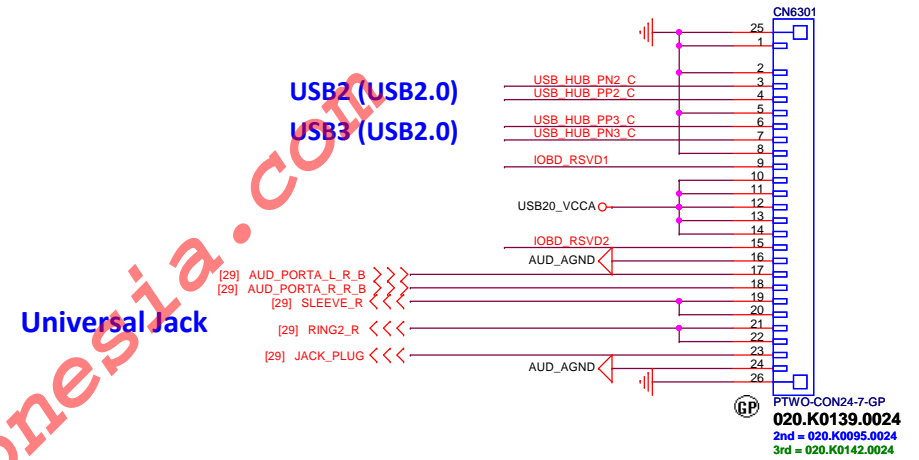
Main Func = IO Connector



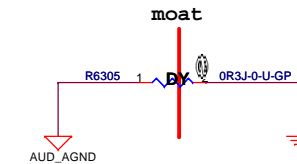
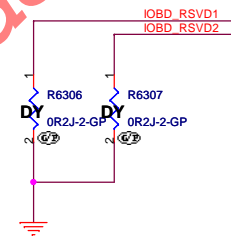
USB2 (USB2.0) CMC

USB3 (USB2.0) CMC

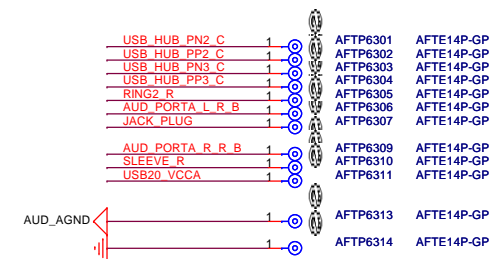
I/O Board Connector



Universal Jack



Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins




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Main Func = Hall Sensor

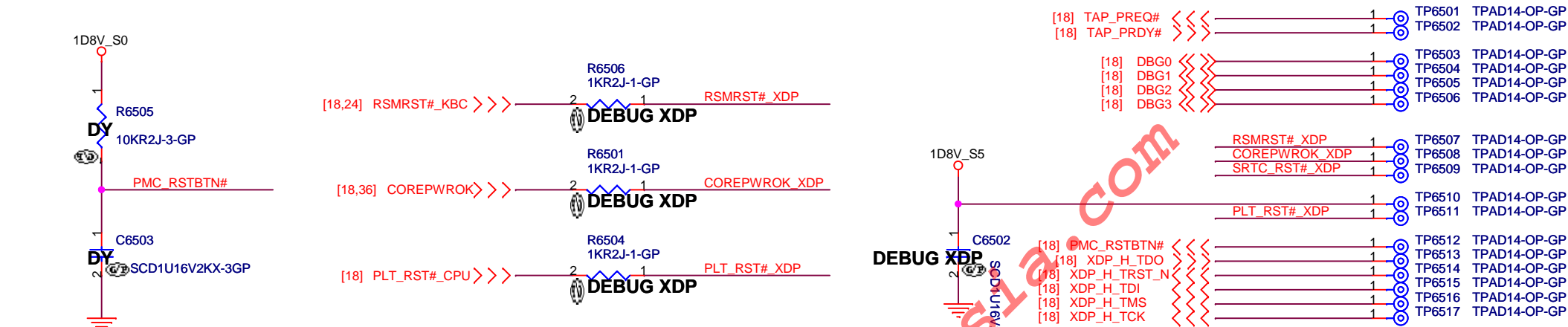
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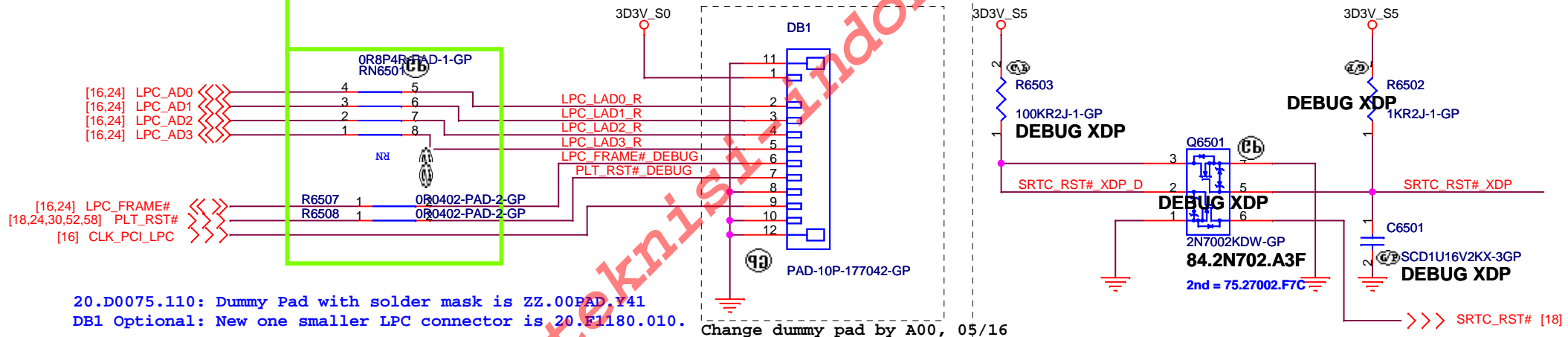
Main Func = Debug



Layout Note:

Place near trace separated point

Debug Connector



Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title			Debug connector	
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Main Func = Sensor Hub+Accelerometer (G-Sensor)+Gyro+Proximity SAR+ALS

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Main Func = G-Sensor

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Main Func = Thunderbolt

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Main Func = dGFX_CORE

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Main Func = dGPU

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Main Func = GFXLCD

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Main Func = GFXCRT

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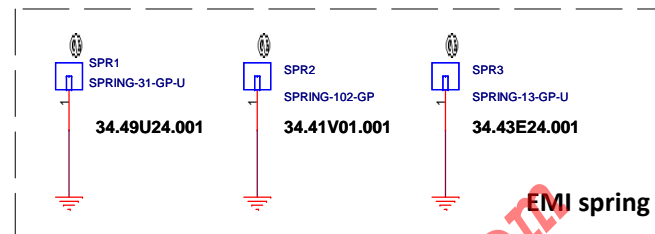
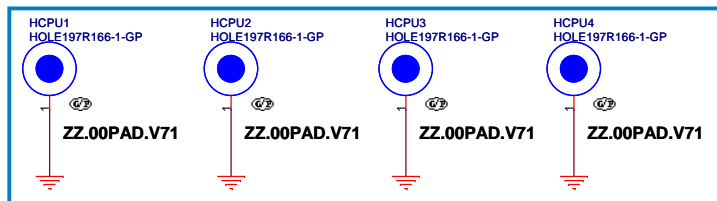
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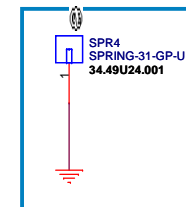
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Main Func = Unused Parts

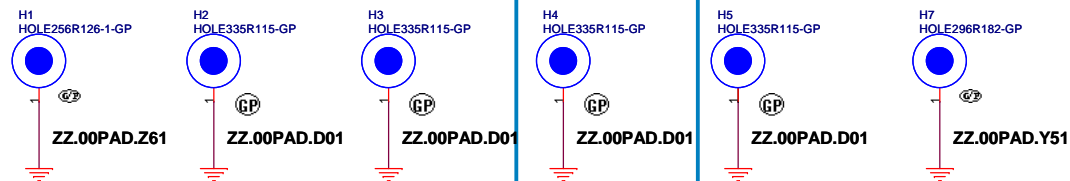
2016.01.14 ME add



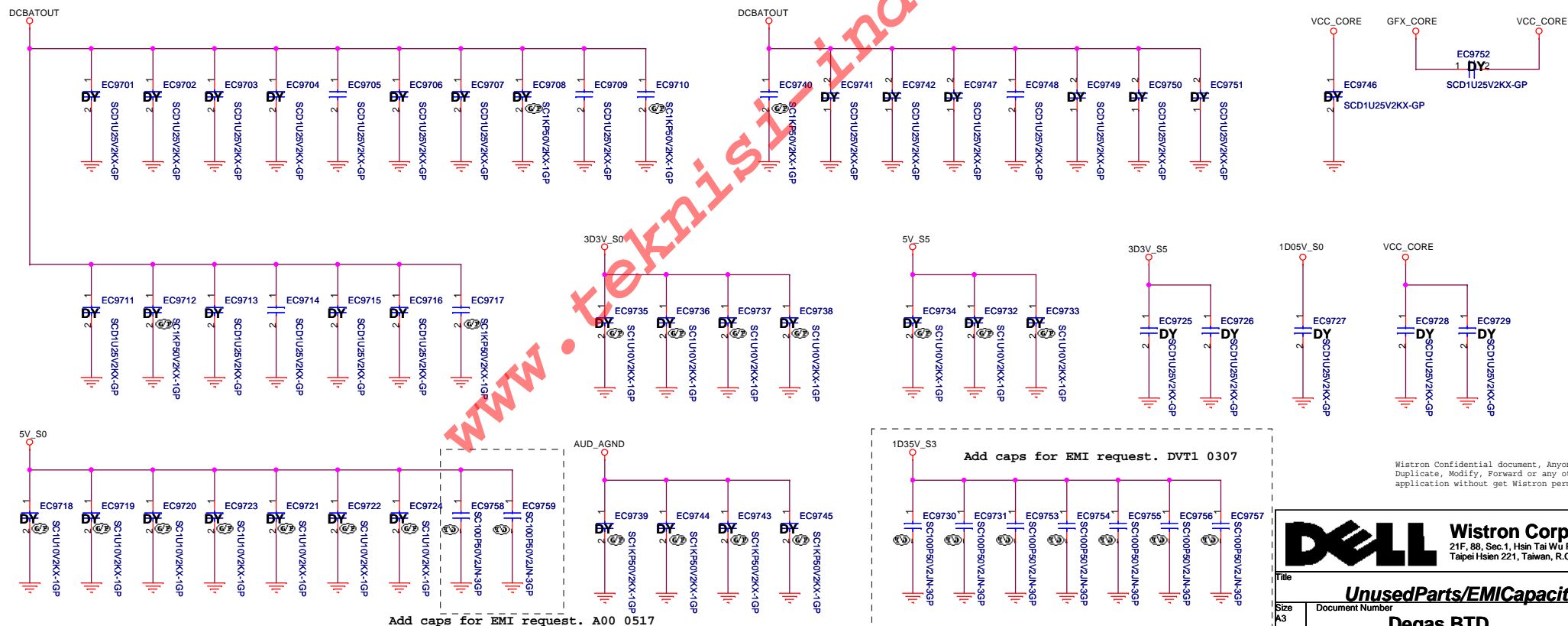
2016.01.14 EMI change



2015.11.16 ME add



Main Func = EMI Capacitors



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Title: **UnusedParts/EMICapacitors**

Size: A3 Document Number: **Degas BTB** Rev: **A00**


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Main Func = NFC

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Main Func = TPM

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Main Func = FPR

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Main Func = SmartCard

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Main Func = SmartCard

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Main Func = Switchable

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Main Func = Dock

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Main Func = LAN

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Main Func = LAN

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Main Func = Debug

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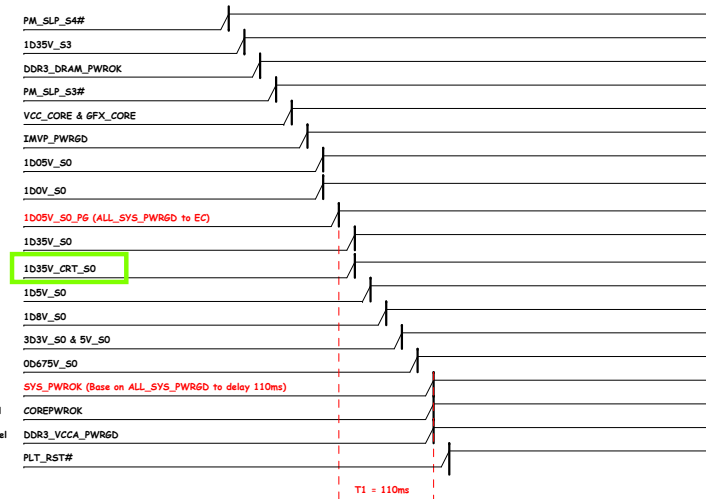
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Ver.	Date	Page	Change Description	Reasons
X01	03/04	16	R1622 R1628 merge to RN1602	RES merge Chip array
X01	03/04	16	R1621 R1624 merge to RN1604	RES merge Chip array
X01	03/04	18	R1804 R1805 merge to RN1801	RES merge Chip array
X01	03/04	18	R1835 R1837 merge to RN1802	RES merge Chip array
X01	03/04	18	R1830 R1855 merge to RN1803	RES merge Chip array
X01	03/04	24	R2401 R2437 merge to RN2405	RES merge Chip array
X01	03/04	53	R5301 R5302 R5303 merge to RN5303	RES merge Chip array
X01	03/04	30	R6111 rename R3002	Schematic page name correct
X01	03/04	18	C1806 C1807 change to 5pF (78.5R074.1FL)	Xtal vendor test report
X01	03/07	52	EC5201,EC5202 change to 33pF for EMI team (78.33034.1FL)	EMI modify
X01	03/07	54	Stuff R5414, R5415, R5416, R5417 for EMI team	EMI modify
X01	03/07	86	Add 100pF caps EC9730,EC9731 EC9753,EC9754,EC9755,EC9756 EC9757 (78.10134.1FL)	EMI modify
X01	03/07	51	Remove PG5107 Reserve PR5116, PR5117.	Reserve 2nd co-layer
X01	03/08	53	Change CRT1 to 020.20107.0015	ME request
X01	03/08	53	Change L5301,L5303,L5305 to 0ohm Dummy C5301 C5304 C5308	CRT EA
X01	03/09	53	Add AFTP	
X01	03/09	24	Change R2424 to 20KohmF (64.20025.L0L)	PCB Version change to SB
X01	03/11	49	Stuff PR4912, PC4920 PC4922 change to 1KpF (78.10224.2FL) PR4902 change to 100KF from 90.9KF (64.11035.L0L)	Power team request
X02	04/15	NA	Change 0 ohm to short pad (0603) L5301,L5303,L5305,R2107,R2405 R2703,R2704,R2711,R2901,R2902 R2903,R2904,R2906,R2907,R2909 R2911,R2914,R3001,R3006,R3016 R3414,R3415,R3624,R3625,R3628 R5212,R5401,R5801,R5802 Change 0 ohm to short pad (0805) R5227,R5601,R5805	part count
X02	04/15	62	Stuff R6226, R6227, Q6206 Q6206 PN change to 84.2N702.A3F from 84.02004.03F	For touch pad discharge schematic
X02	04/15	34 63	EU3401, TR6302 to 075.09904.0A7C TR6301, TR6302 change to 68.01012.20B	EMI request
X02	04/18	24	R2424 change to 33kR-F	DVT2 PCB version
X02	04/18	11,12 42-50	Change some 0R to shortpad Change PC4201 to popular part (P/N: 78.10594.41L)	Power team modify
X02	04/18	47	PT4701 change P/N to 79.33612.6CL	For acoustic noise
A00	05/16	24	R2424 change to 64.9k by A00 PCB version	PCB Version change to A00
A00	05/16	NA	Change 0 ohm to short pad (0402) R1608,R1611,R1614,R1615,R1616 R1818,R1823,R1827,R1828,R1832 R1836,R1923,R1924,R1925,R1929 R2102,R2104,R2105,R2402,R2407 R2412,R2414,R2416,R2422,R2429 R2430,R2434,R2441,R2449,R2453 R2458,R2460,R2461,R2465,R2467 R2507,R2613,R2701,R2702,R2705 R2714,R2716,R2718,R2719,R2720 R3005,R3403,R3404,R3405,R3406 R3421,R3422,R3423,R3611,R3614 R3619,R3626,R3627,R3665,R3703 R4301,R5201,R5225,R5232,R5304 R5305,R5406,R5407,R5408,R5409 R5410,R5411,R5412,R5413,R5604 R5809,R5815,R6104,R6105,R6202 R6214,R6218,R6223,R6224	part count
A00	05/16	52	Change DB1 to dummy pad	
A00	05/17	86	Add EC9758 EC9759(78.10134.1FL) Stuff SPR1 (34.49024.001)	EMI request

[illegible]

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Timing diagram for the R5M reset sequence. The diagram shows the relationship between several signals: RTC_AUX_S5, RTC_RST#, 3D3V_AUX_S5, ECRST#, S5_ENABLE / 3V_5V_EN, 5V_S5 / 3D3V_S5, 3V_5V_POK, 1DOV_S5, 1DOV_S5_P6, 1D8V_S5, 1D8V_S5_P6, and R5MRST#_KBC. A red dashed vertical line marks the start of the reset sequence. A red arrow indicates a 60ms delay from the S5_ENABLE signal to the R5MRST#_KBC signal. A red label $T1 = 60\text{ ms}$ is shown at the bottom.

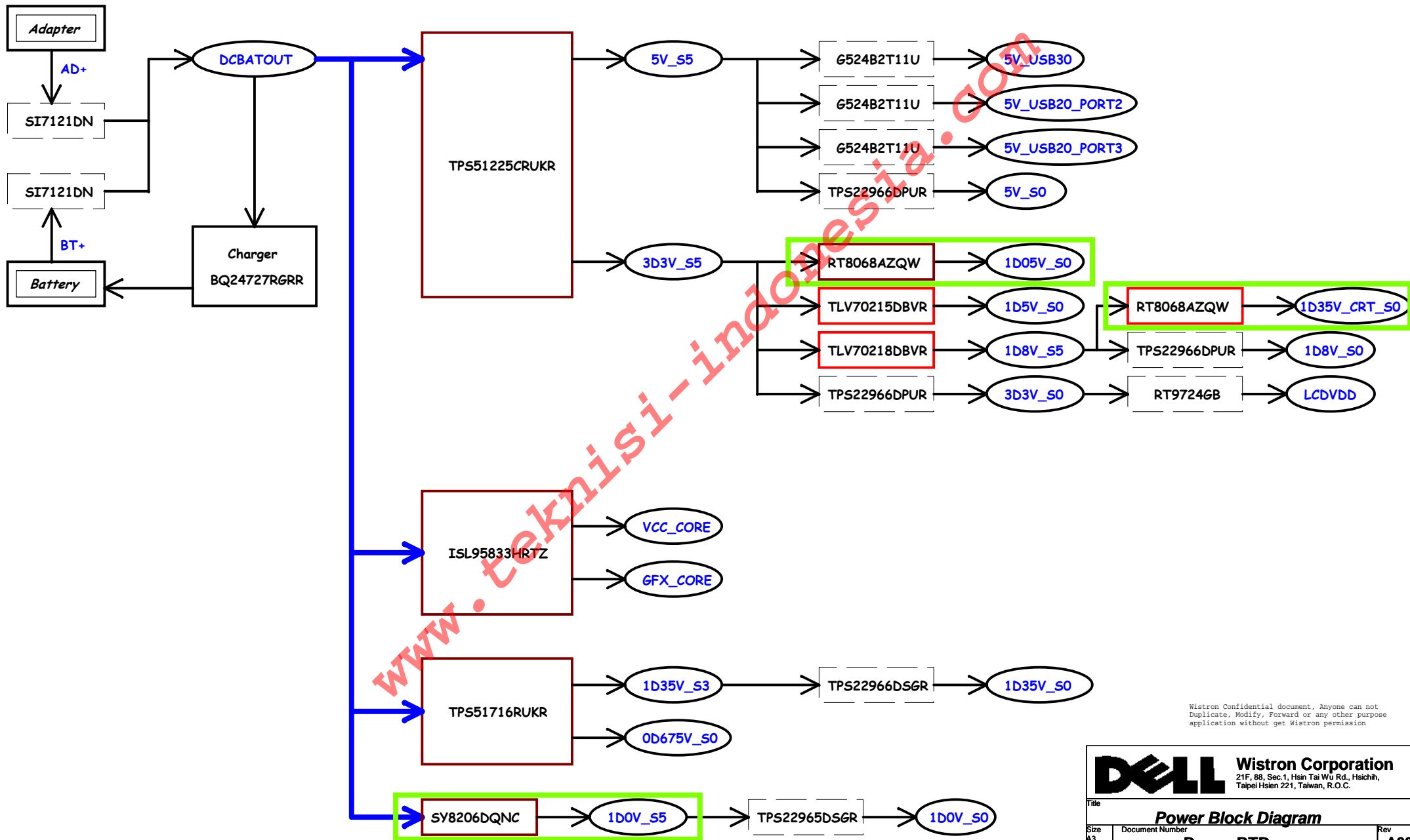


Power IC Type

Regulator

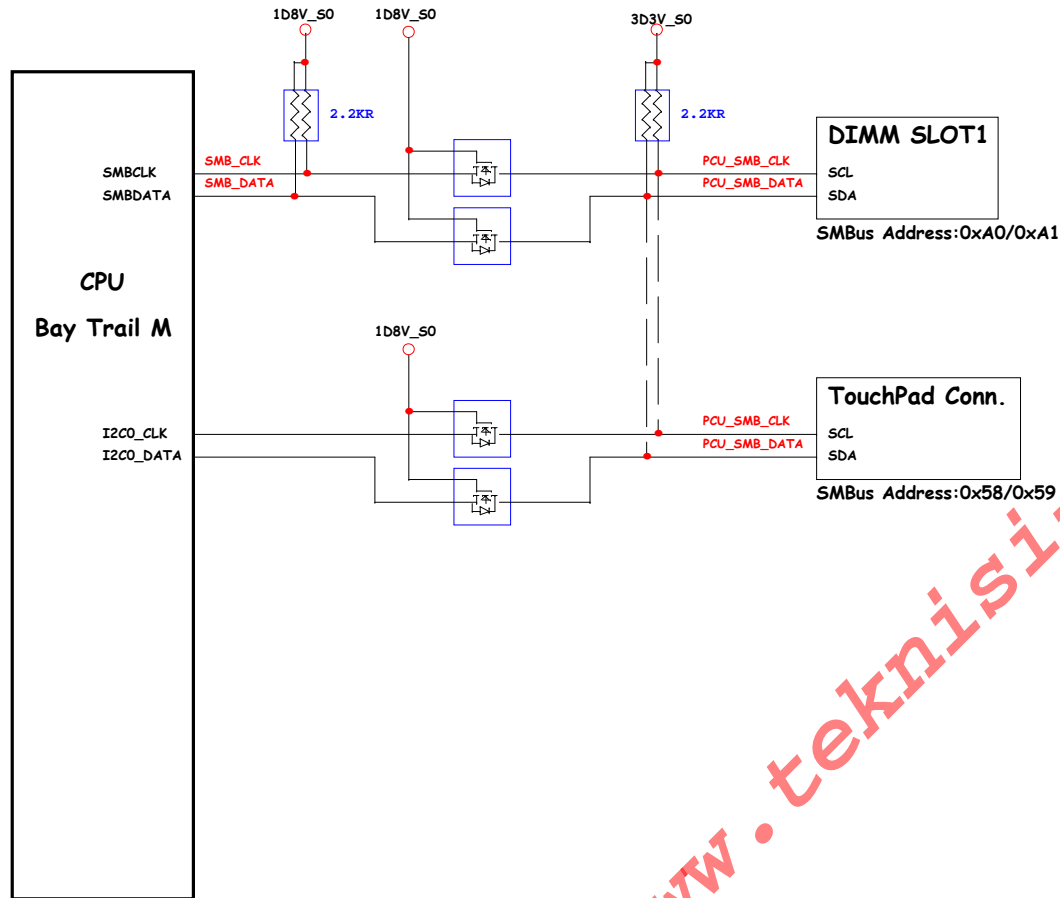
LDO

Load
Switch

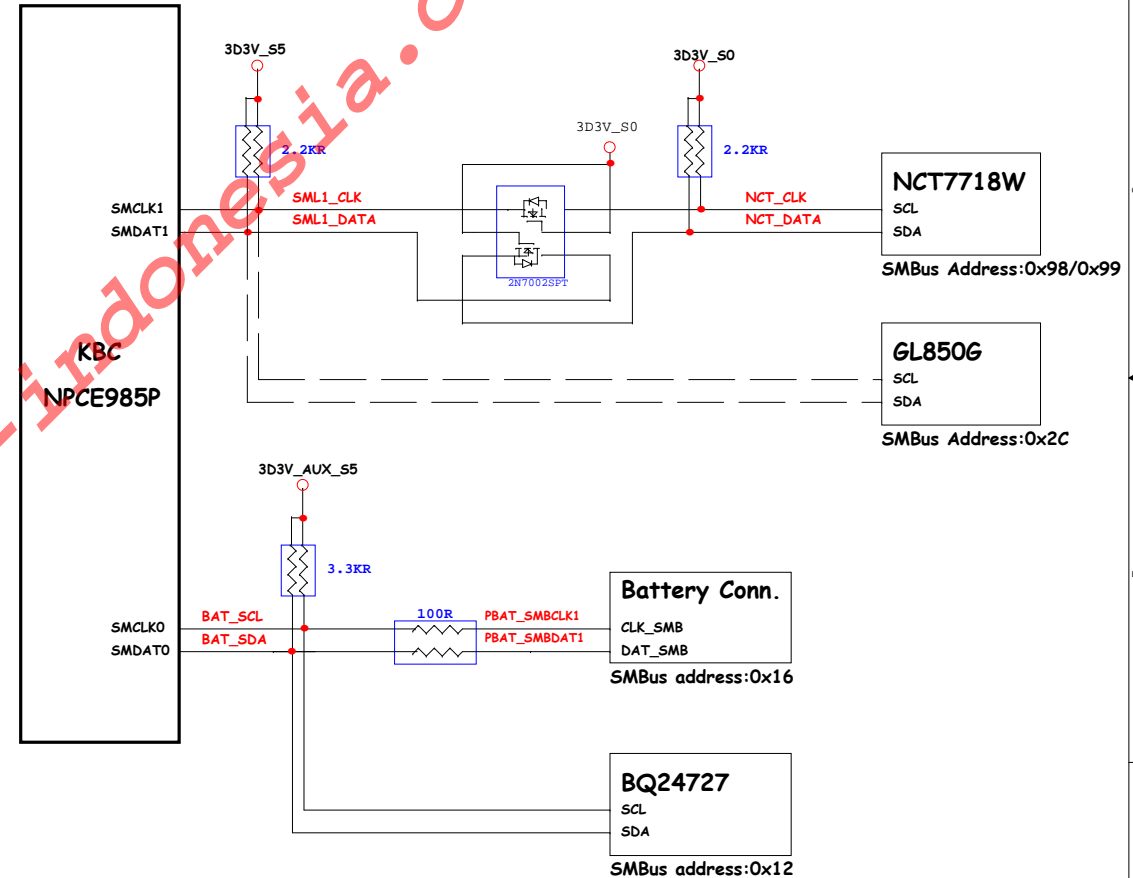


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CPU SMBus / I2C Block Diagram

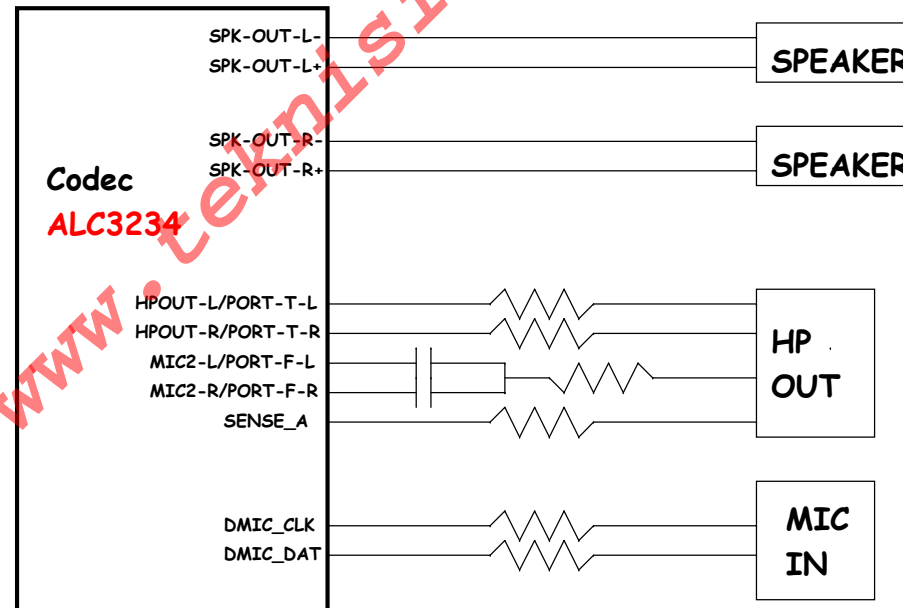
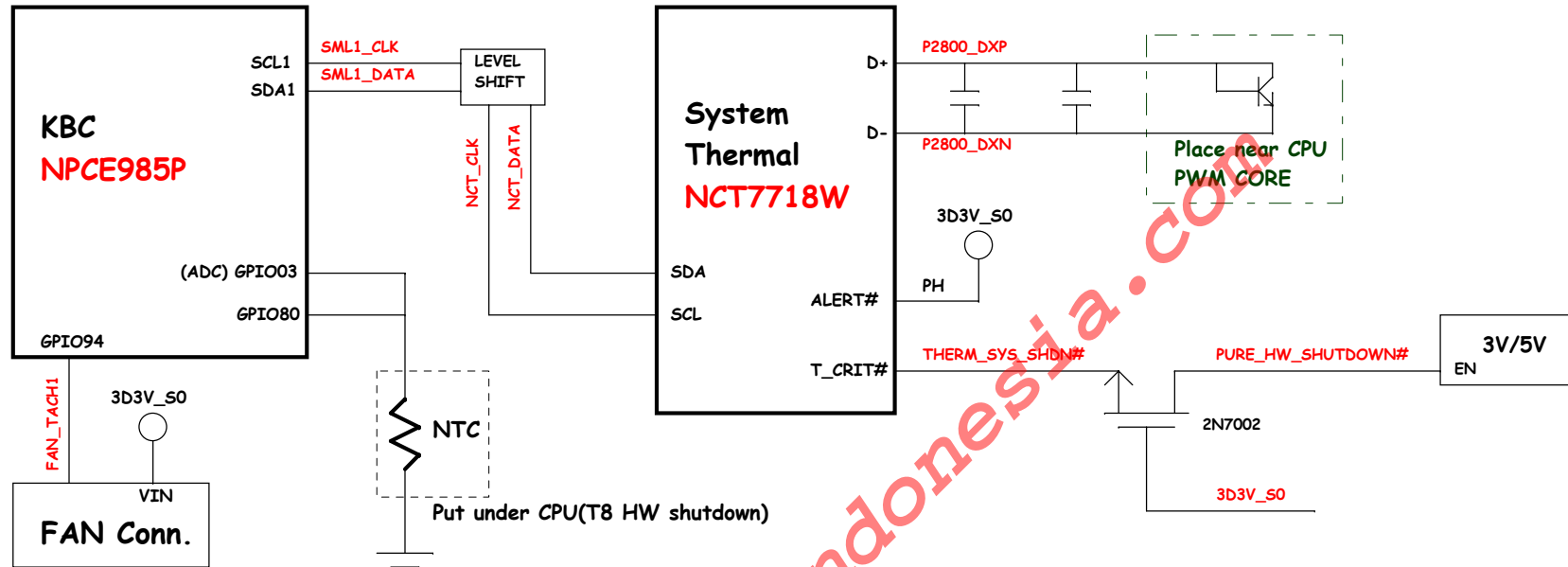


KBC SMBus Block Diagram



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Audio Block Diagram



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